Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation

Daisuke Kosaka, Makoto Nagata

Department of Computer and Systems Engineering
Kobe University

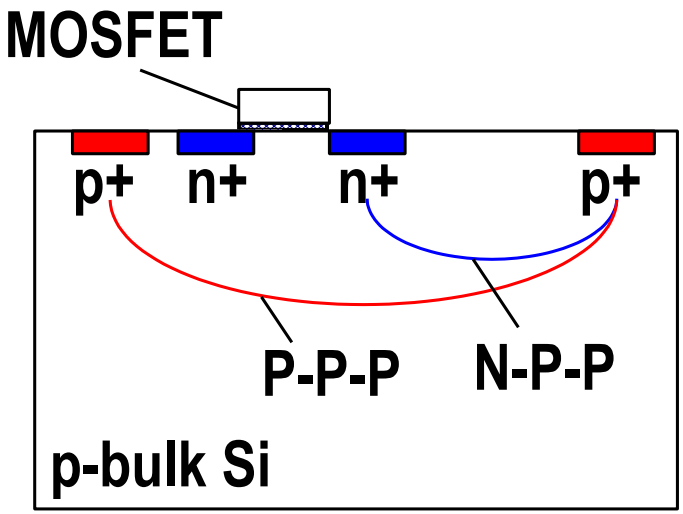
Outline

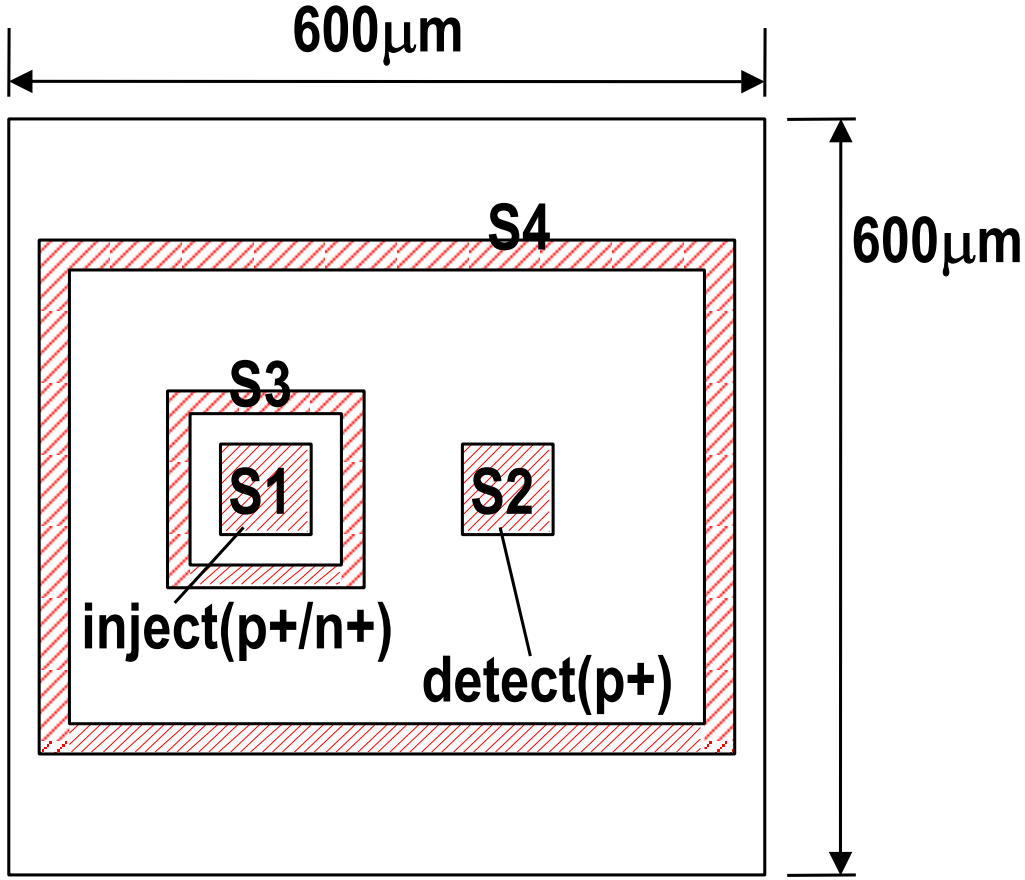
- Motivation
- RF substrate coupling paths and isolation strategies in CMOS technology
  - Btwn. MOSFETs, ground wiring to substrate
  - p+/n+ guard ring, deep n-well(DNW)
- Substrate equivalent circuit modeling technique
  - Test structure for 2-port S21 evaluation
  - F-matrix modeling and analysis
  - Short/cut of observation points, 3-sub-model stack
- Summary

Motivation

- **Substrate crosstalk**
  destructive to analog/RF circuit design for SoC
- **Substrate coupling isolation strategies**
  p+/n+ guard ring, deep well are effective?
- **Precise modeling/simulation of isolation structures**
  requisite tool for layout/device level modeling

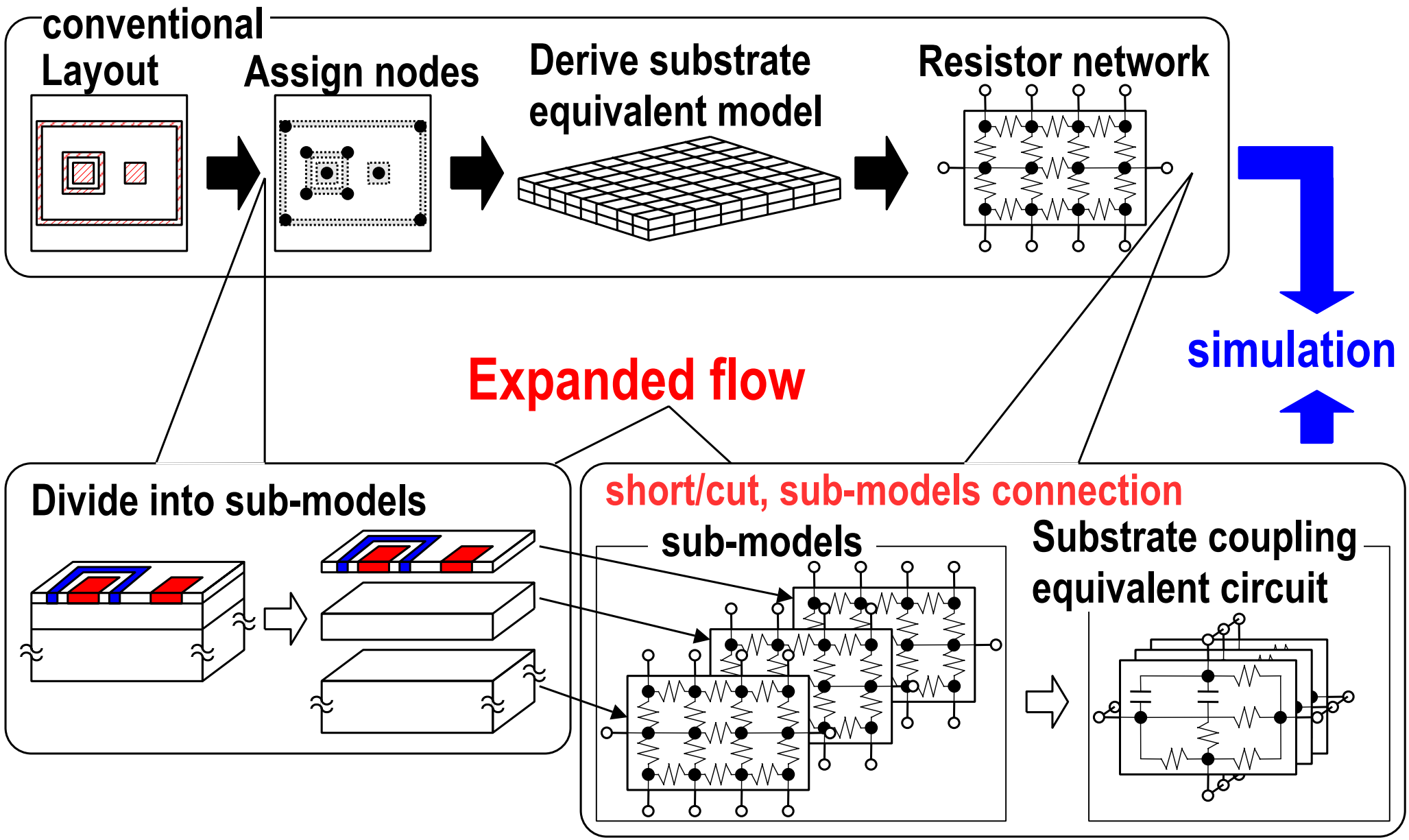
Substrate coupling and test structure



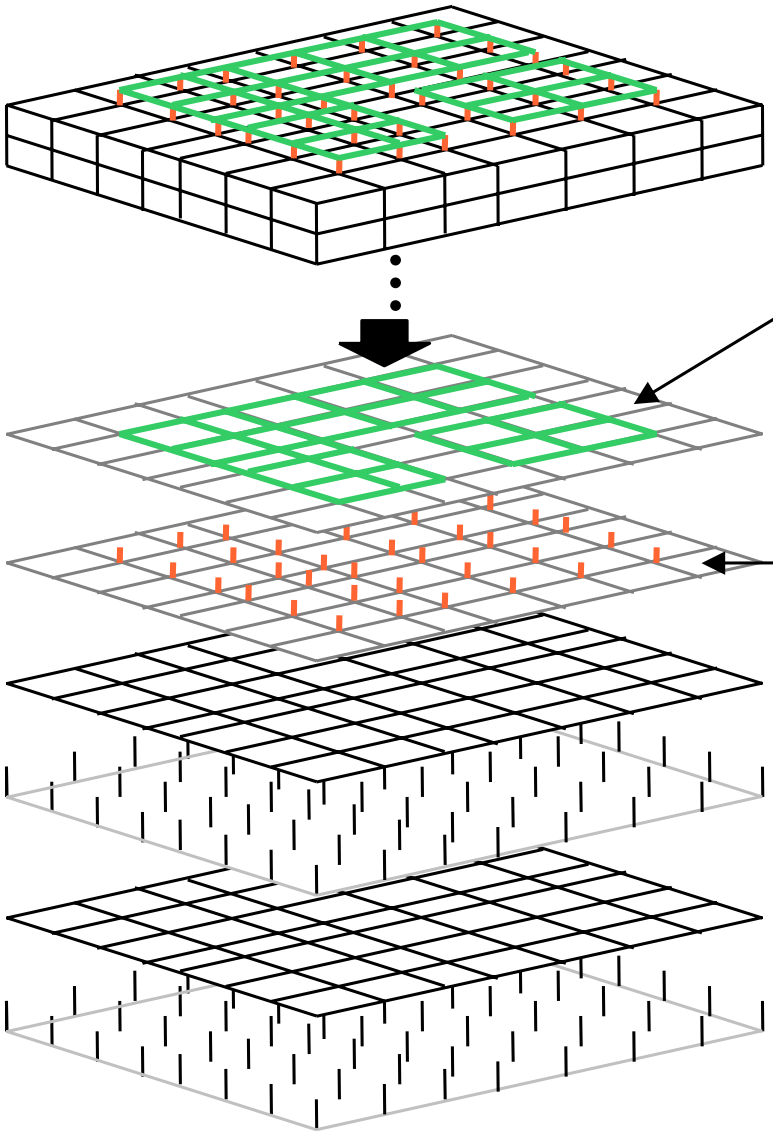


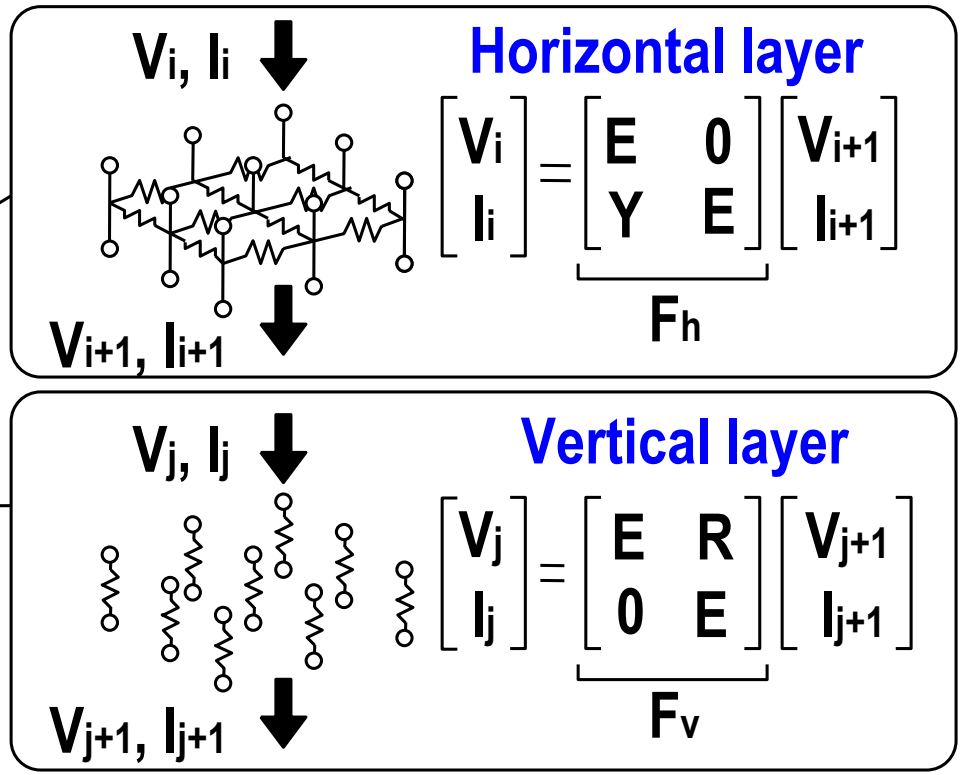
- PPP: Btwn. substrate contacts at different locations
- NPP: source/drain junction of NMOS to substrate

Equivalent circuit modeling flow



Chip-level F-matrix cascade (Murasaka, ISQED'01)

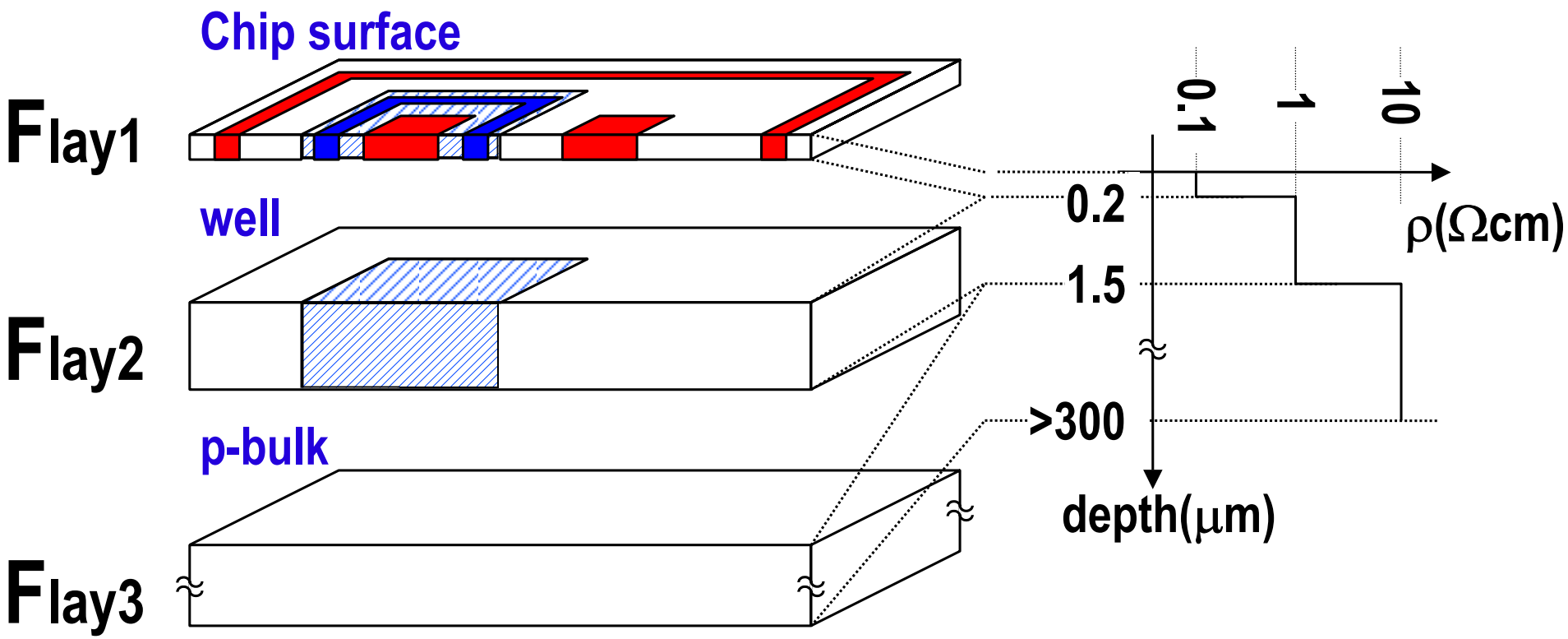




$$\begin{bmatrix} V_{top} \\ I_{top} \end{bmatrix} = \underbrace{F_h F_v}_{\text{Wiring}} \underbrace{F_h F_v F_h F_v}_{\text{Substrate}} \cdot \begin{bmatrix} V_{btm} \\ I_{btm} \end{bmatrix}$$

3-sub-model stack

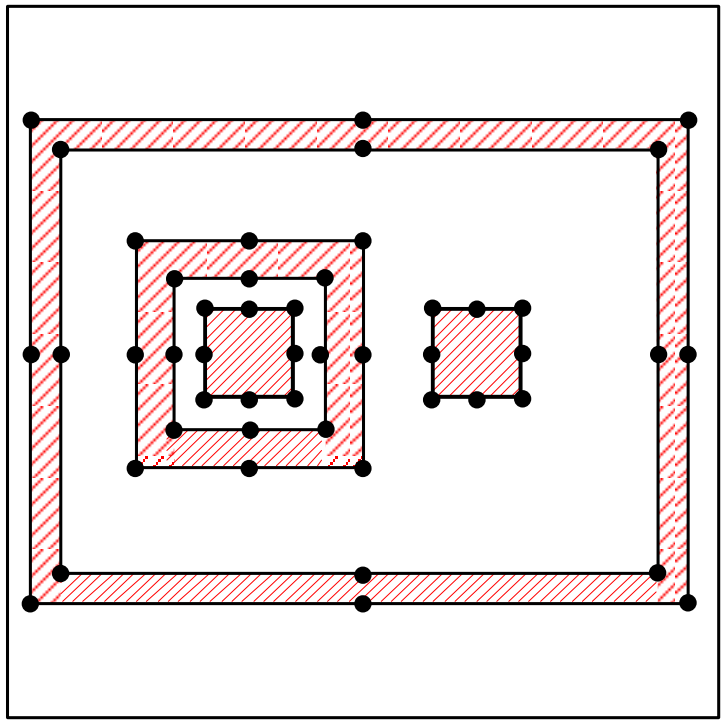
- Assumed impurity profile in Si substrate



$$F_{multi} = F_{lay1} * F_{lay2} * F_{lay3}$$

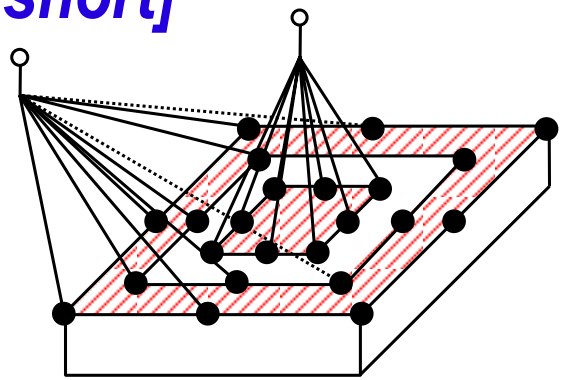
Assignment and short/cut

- Expressing diffusion pattern and polarity



■ Assign observation points around S1, S2, S3 and S4

[short]

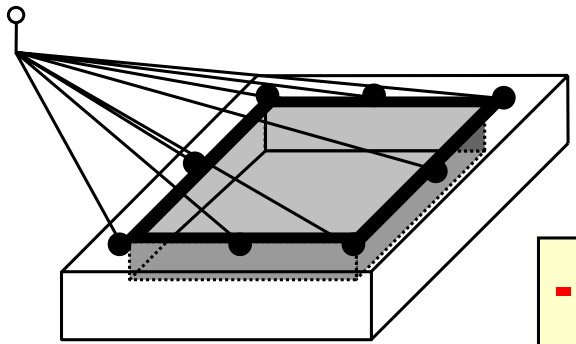


Covered by highly conductive sheet

↓

- short together and provide a single port

[cut]

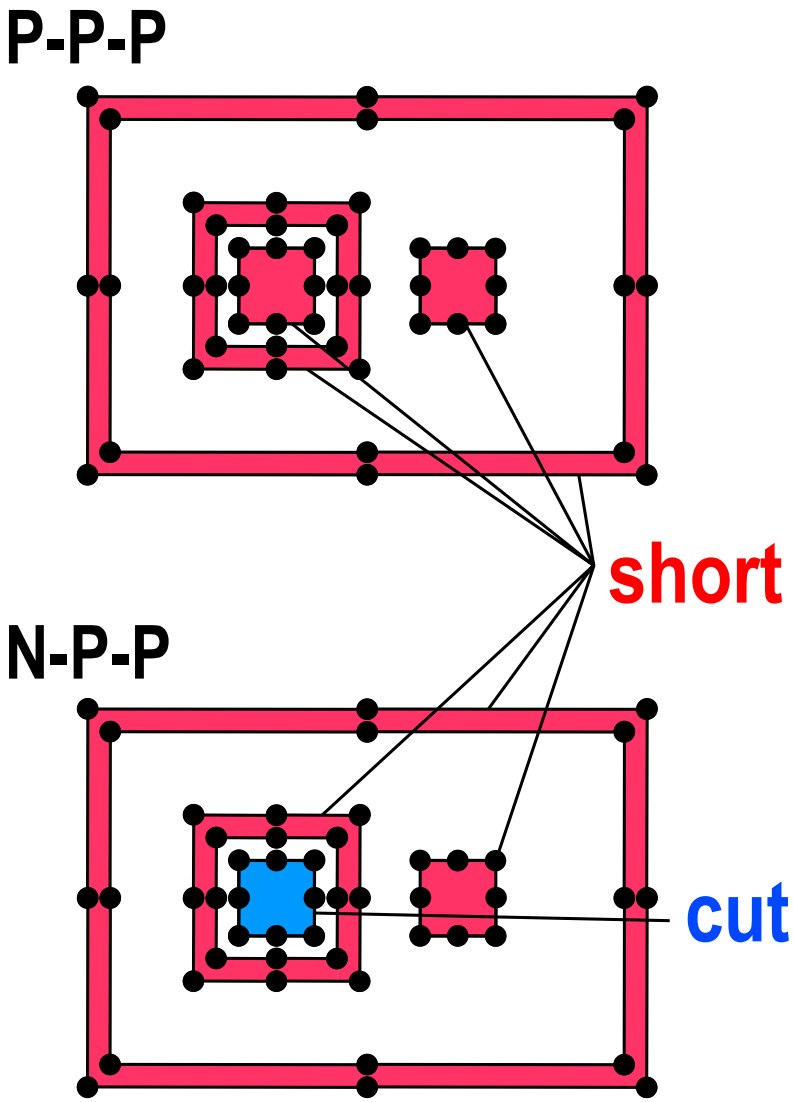


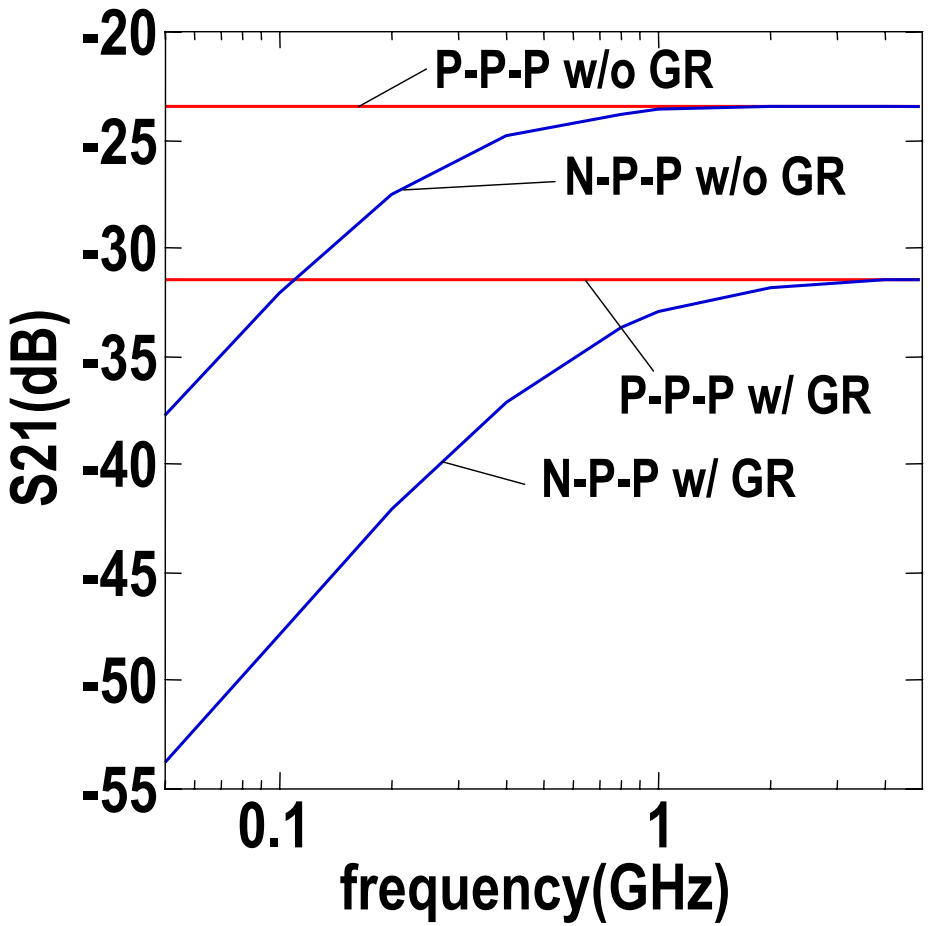
Covered by junction capacitance

↓

- cut observation points within each of the areas
- unite to another single port facing the bulk

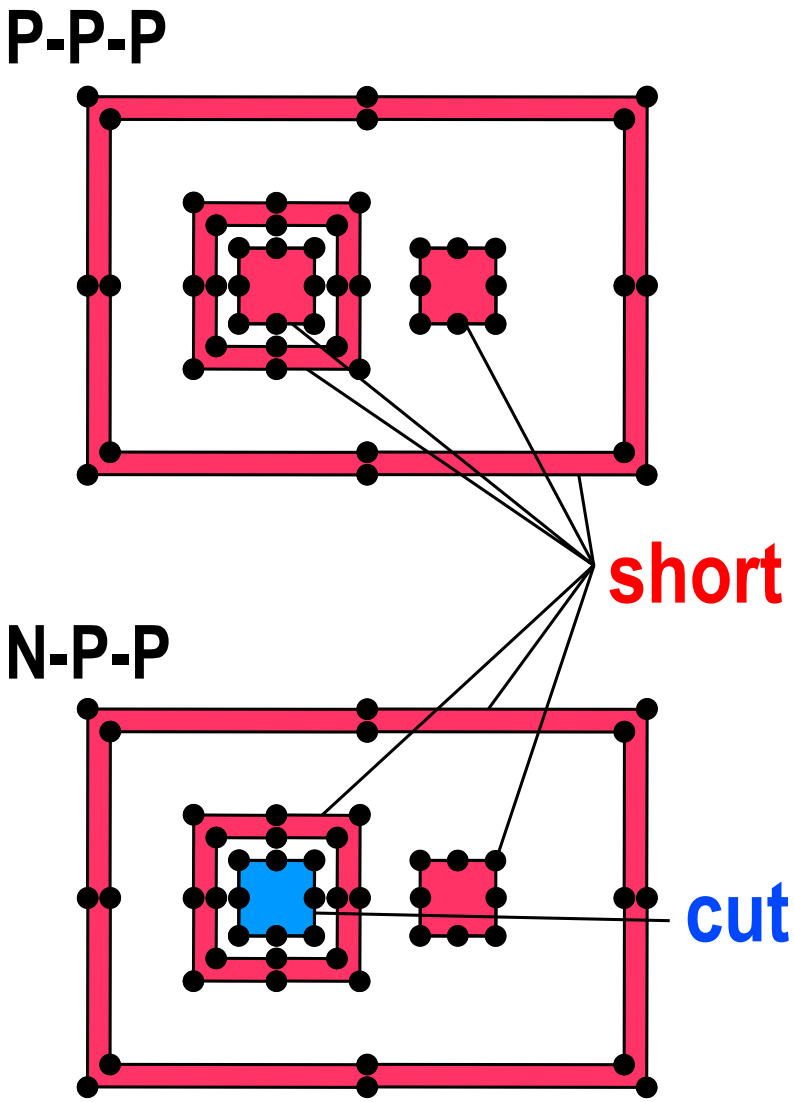
Simulated S21 vs. frequency

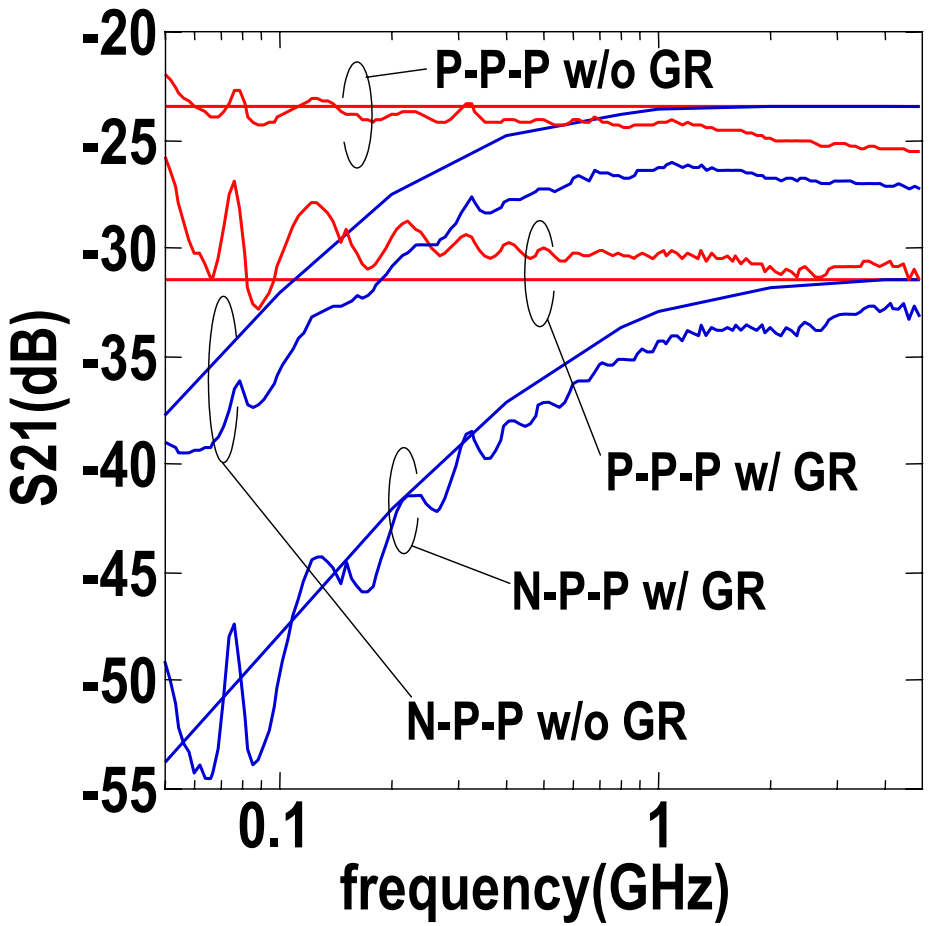




- Standard 0.25-μm CMOS

Comparison with measurements

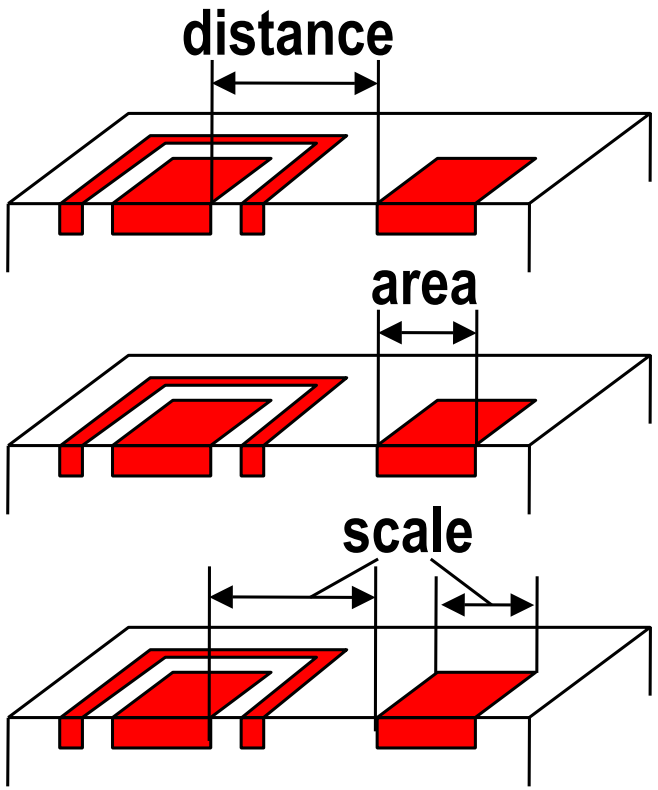


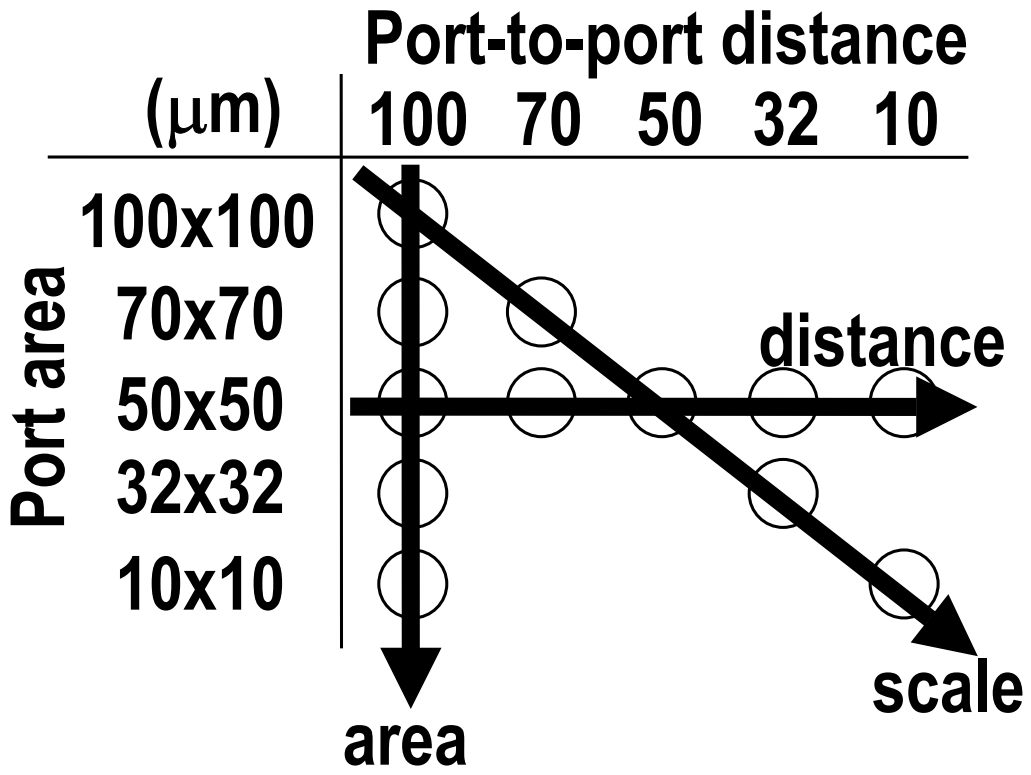


- Standard 0.25-μm CMOS

Layout dependency

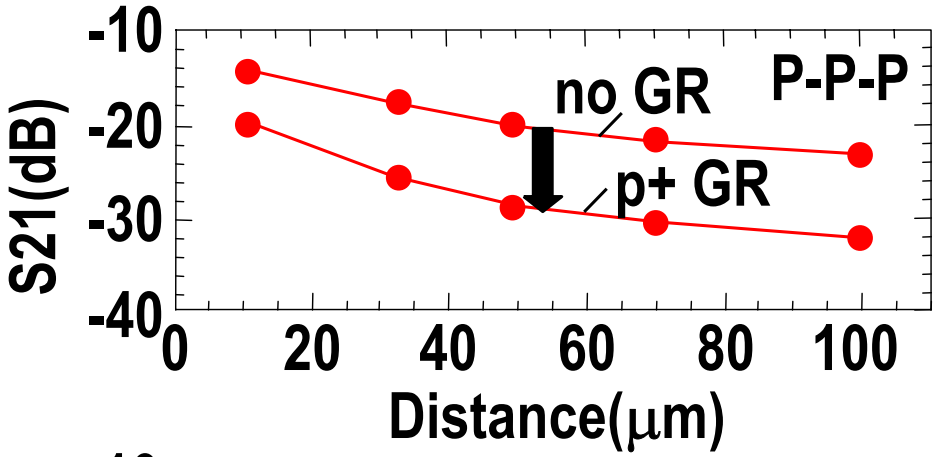
- Standard 0.25-μm CMOS fabrication process
- p+ guard ring

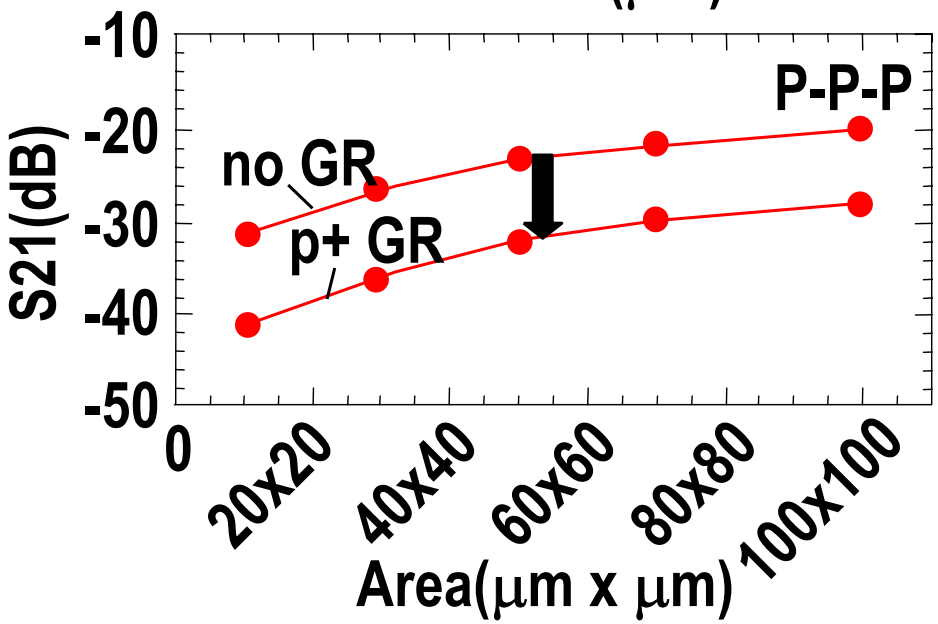




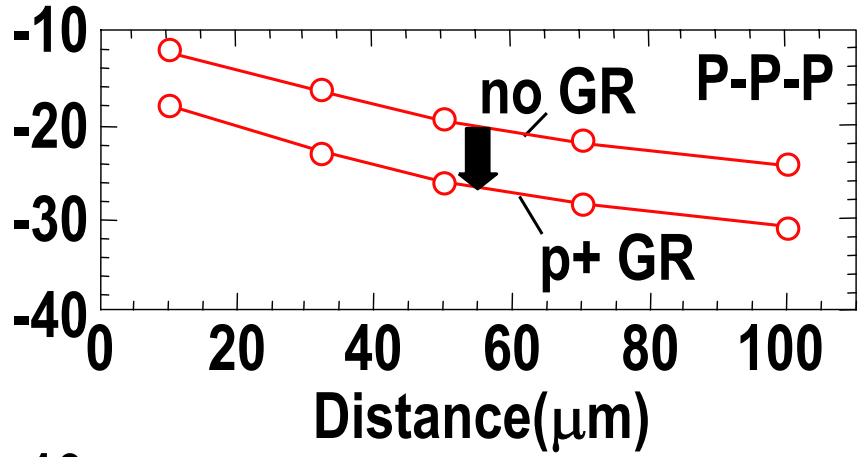
Layout dependency — Results

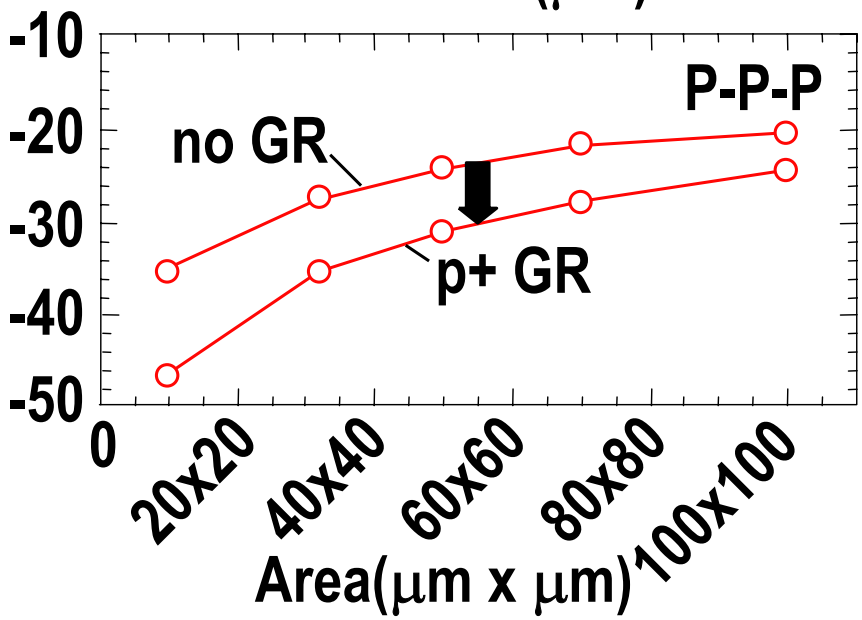
Simulation





Measurement





Analysis time

Modeling condition

analysis area	600μm x 600μm
number of meshes in x/y direction	240/240
total number of meshes in z direction	13
total nodes in mesh	755053
assigned nodes	48
number of terminals in derived model	648

CPU running time

step	time(sec)
assignment observation points	300
F-matrix operation	1800
short/cut, connect sub-models	30
simulation (SPICE)	30~120

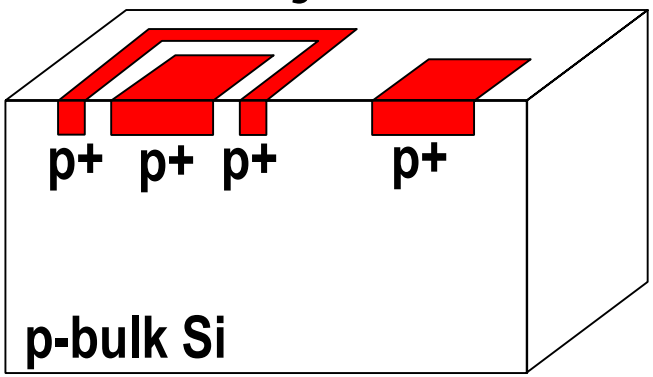
Further modeling is needed

- **Analysis of known structures with F-matrix computation**
  measurements and simulation : consistent
  layout dependency : consistent

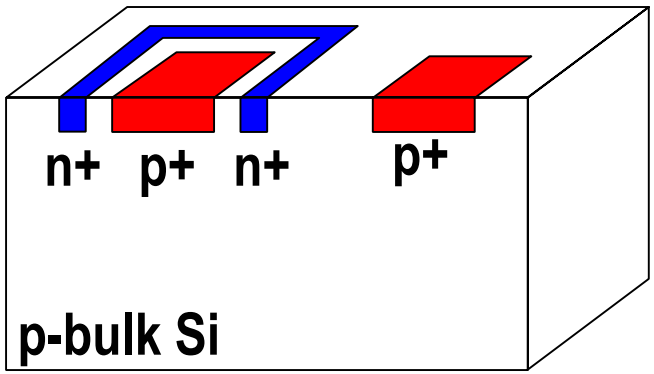
- **Enabled to analyse unknown guard ring structures**

Substrate coupling isolation strategies

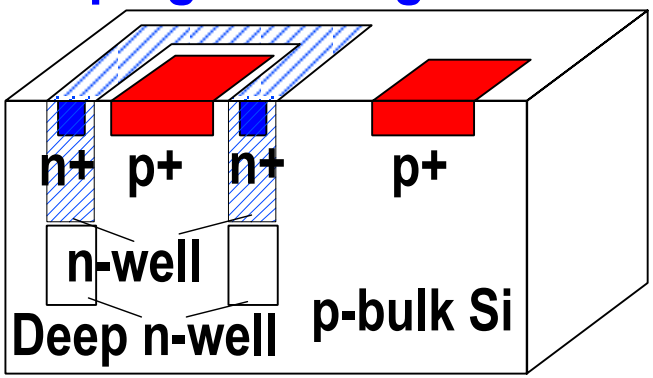
- Absorb and drain out, cut and force to detour current flowing at the substrate
- Different junction capacitance



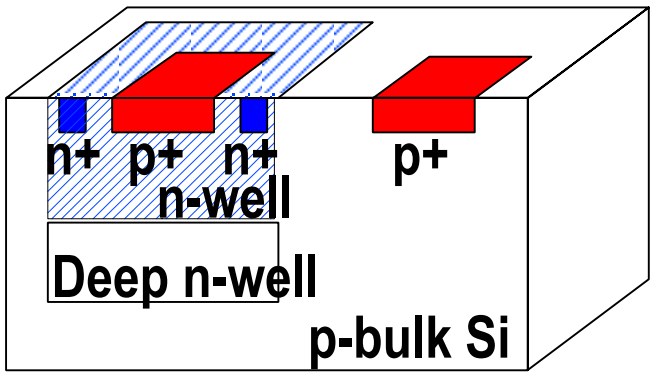
p+ guard ring



n+ guard ring



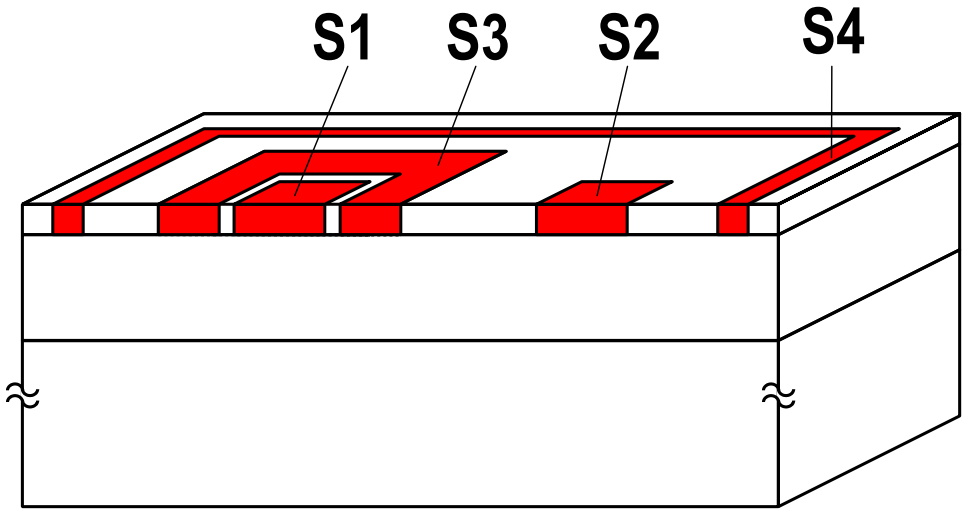
deep n-well guard ring

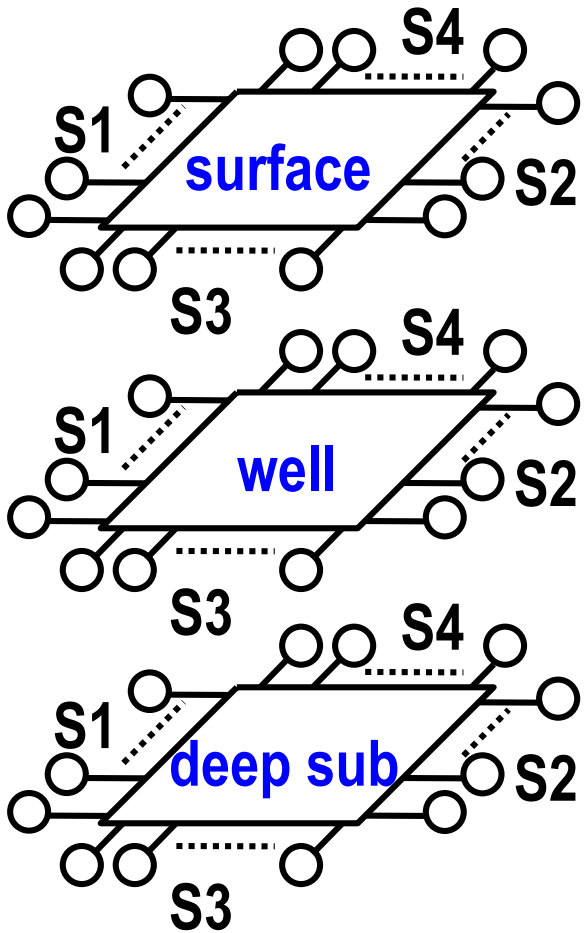


deep n-well pocket

p+ guard ring

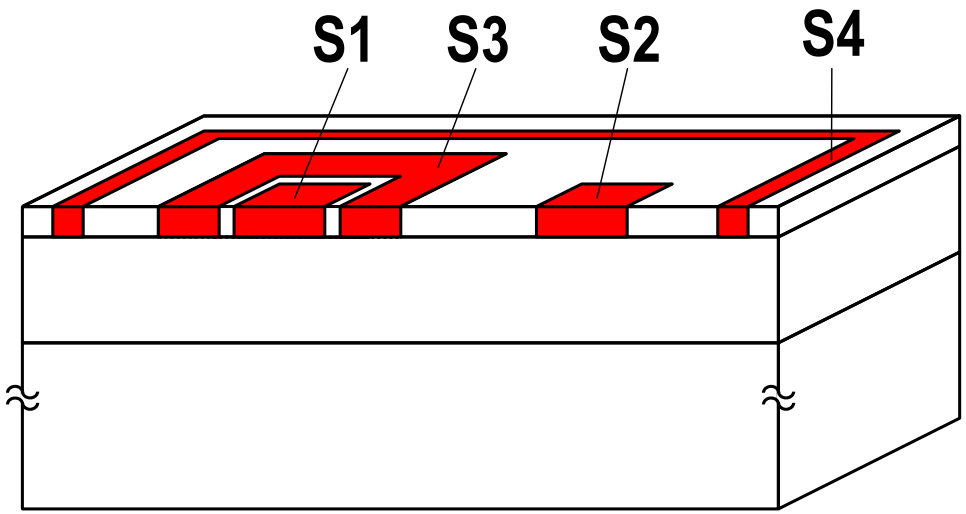
- Derive sub-models

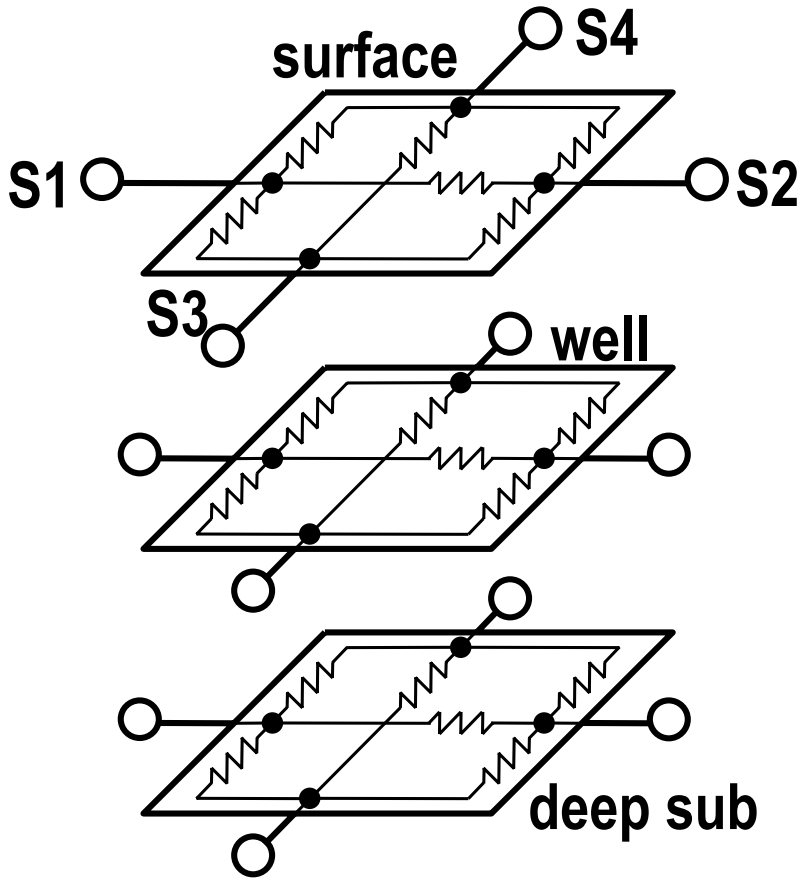




p+ guard ring

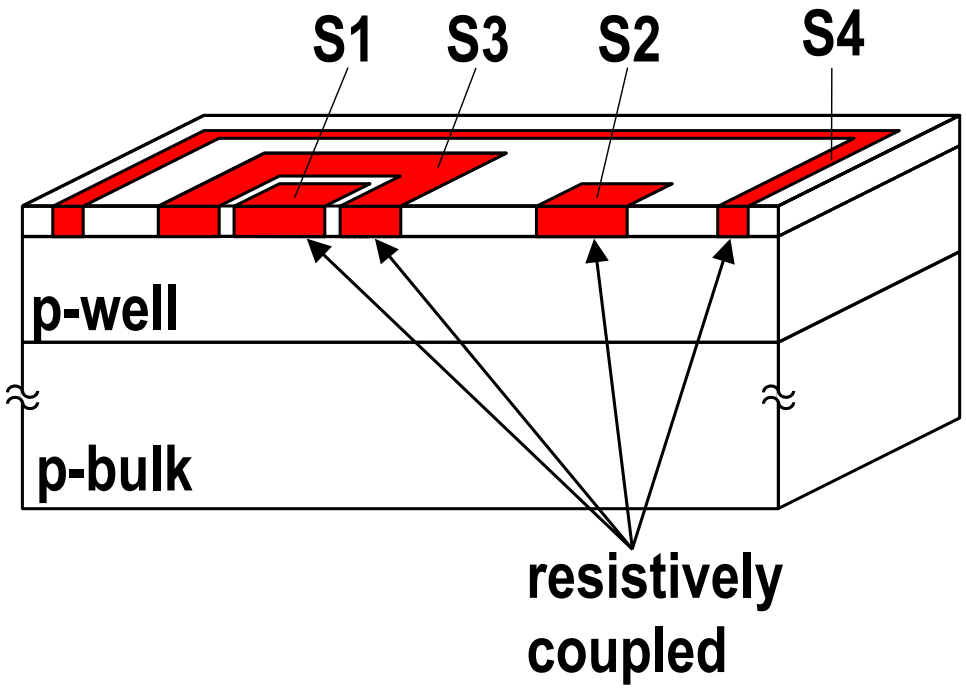
- Short observation points

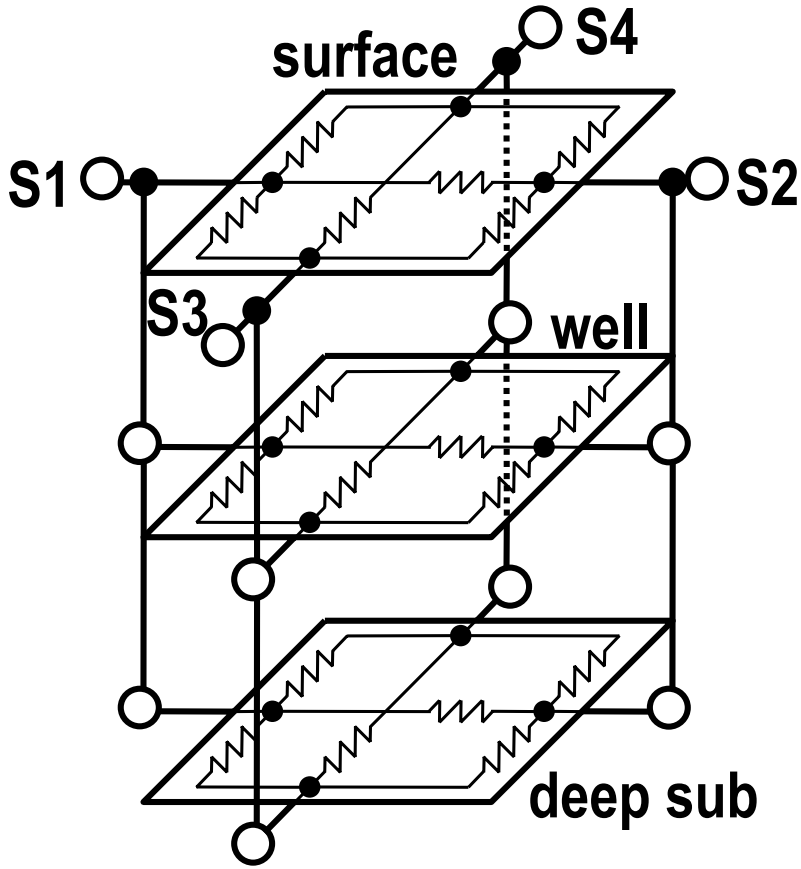




p+ guard ring

- Connect sub-models

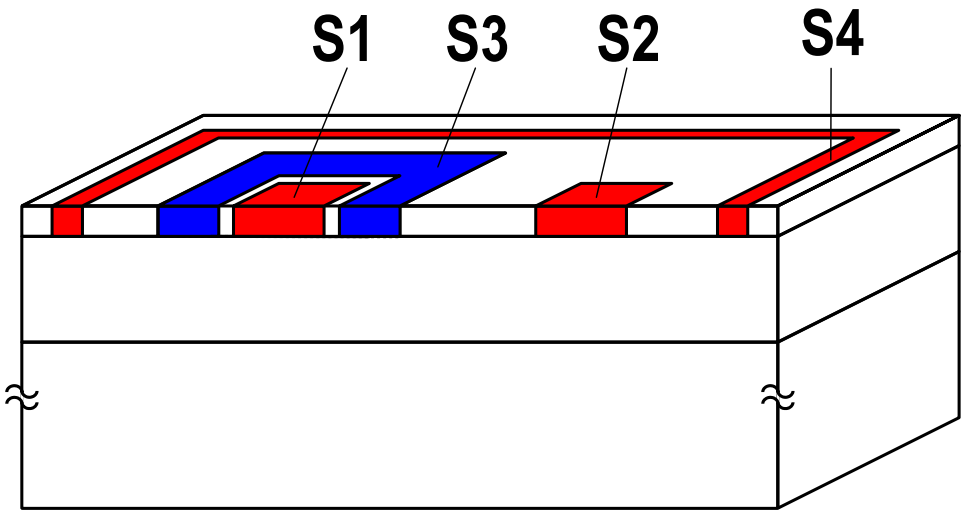


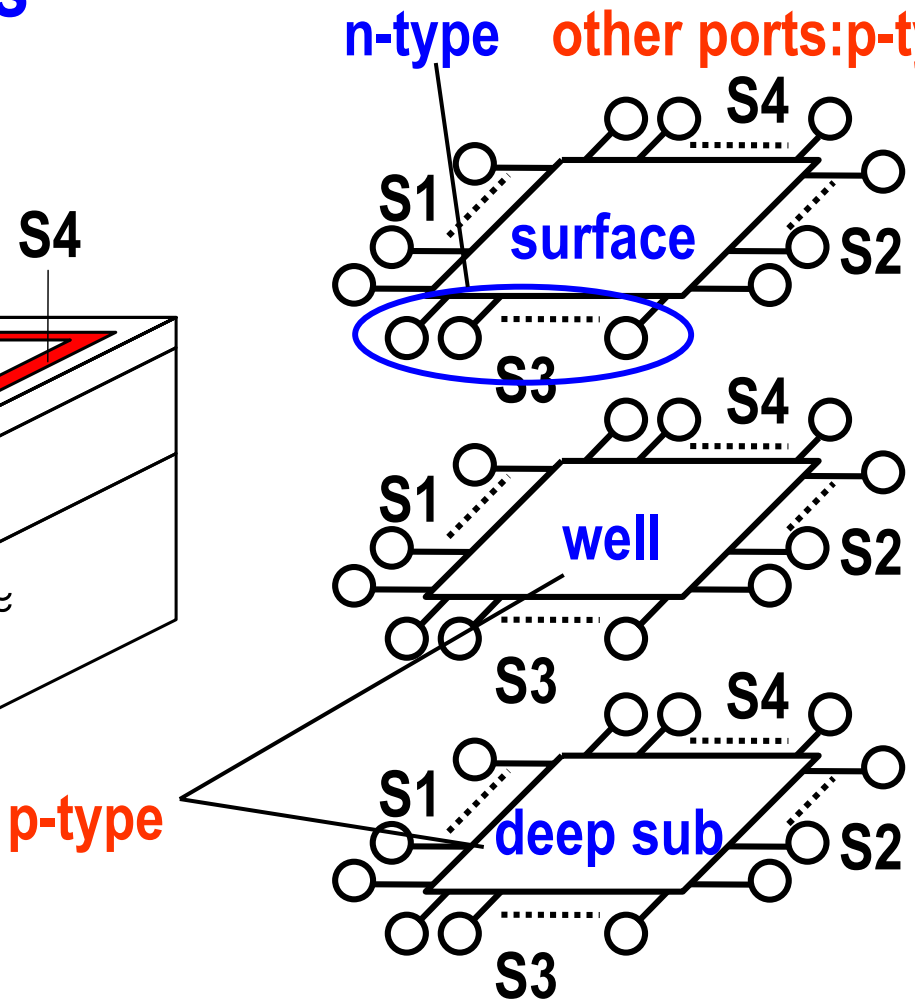


- Sub-models : connected without intermediate elements

n+ guard ring

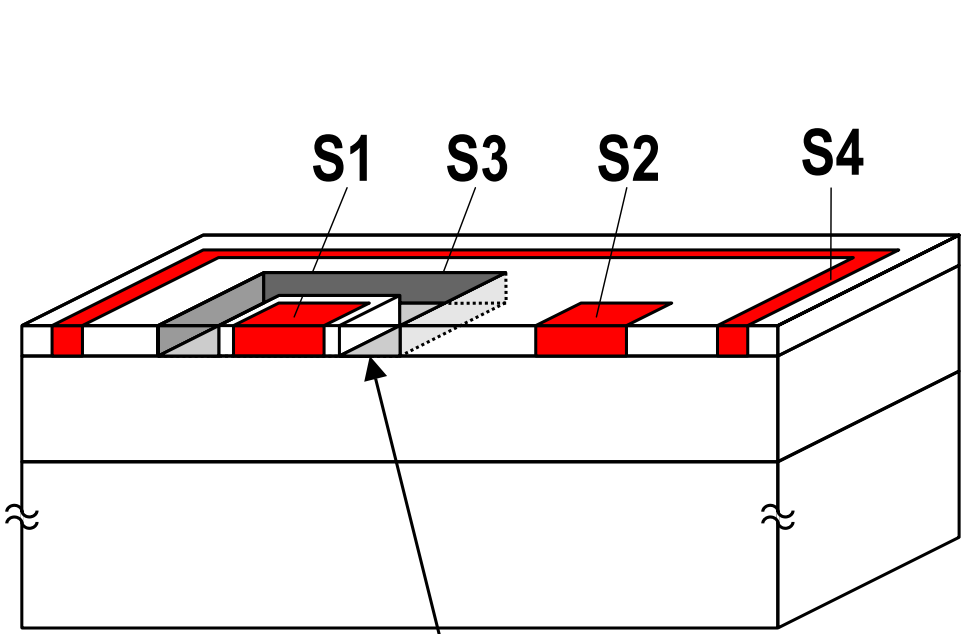
- Derive sub-models

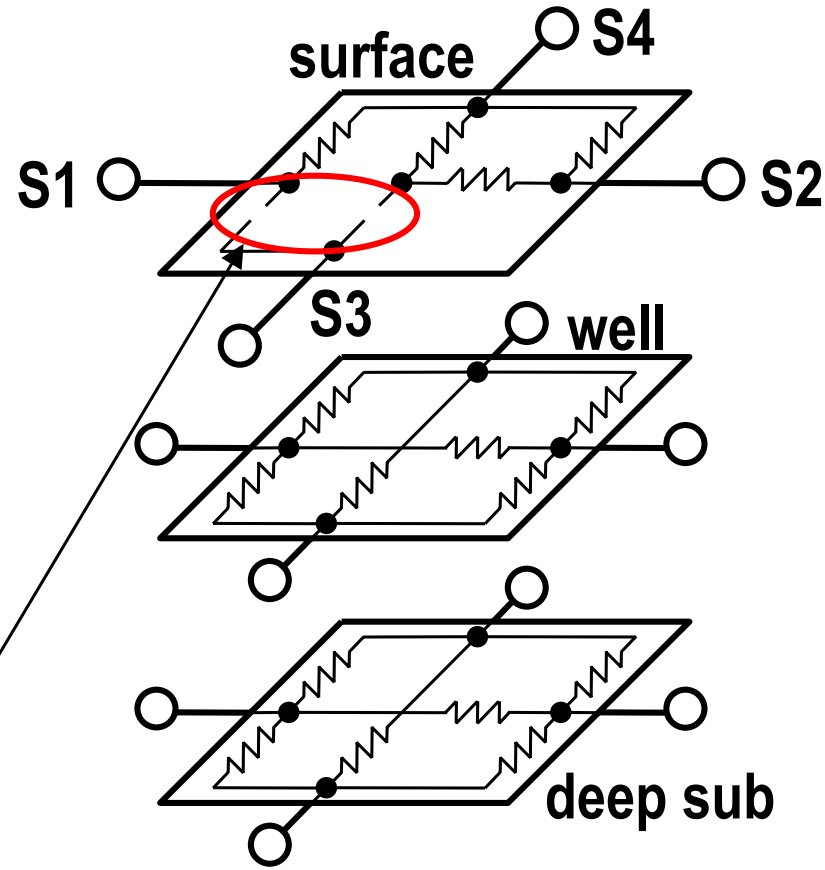




n+ guard ring

- Short/cut observation points

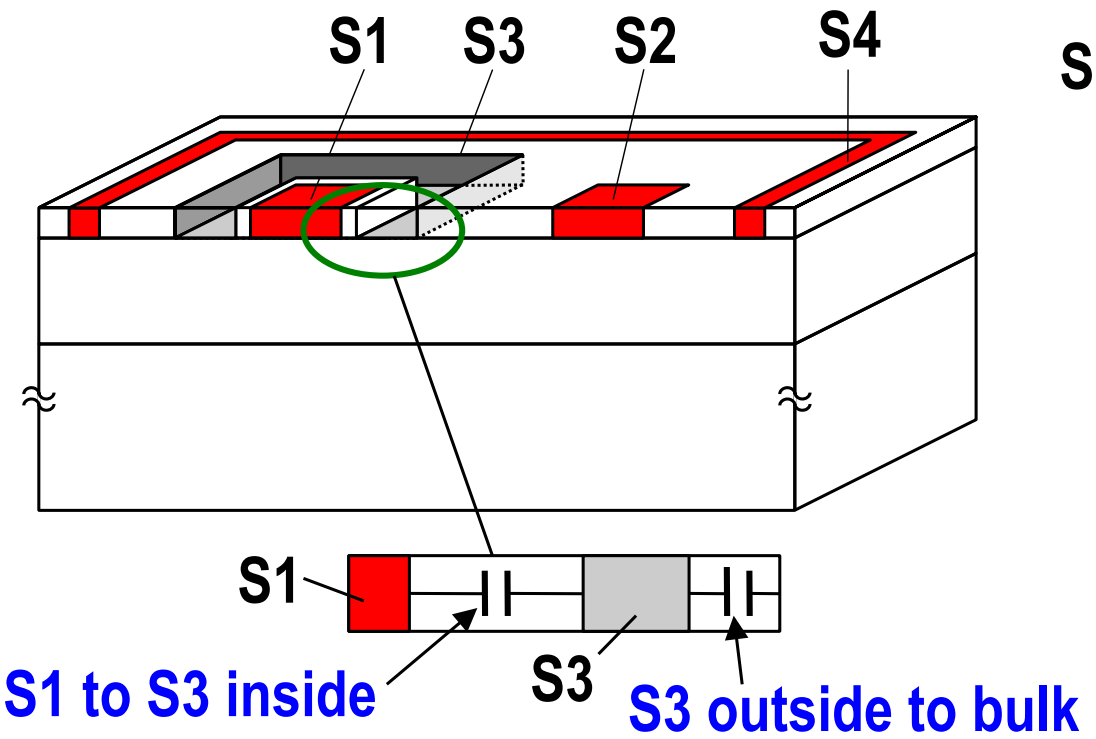


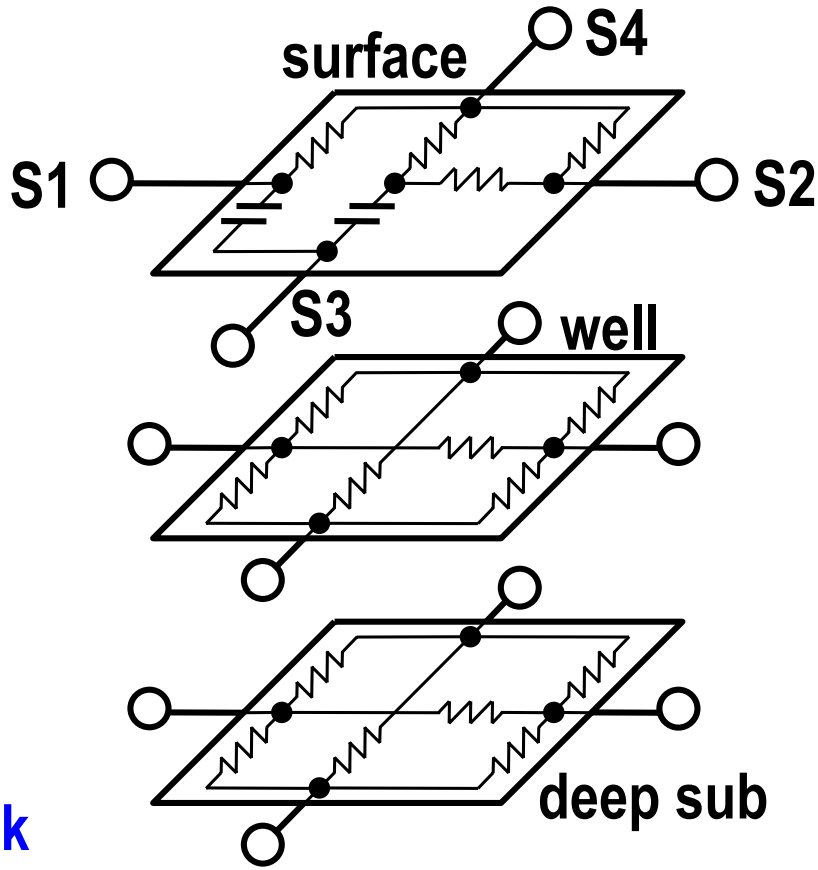


Cut observation points

n+ guard ring

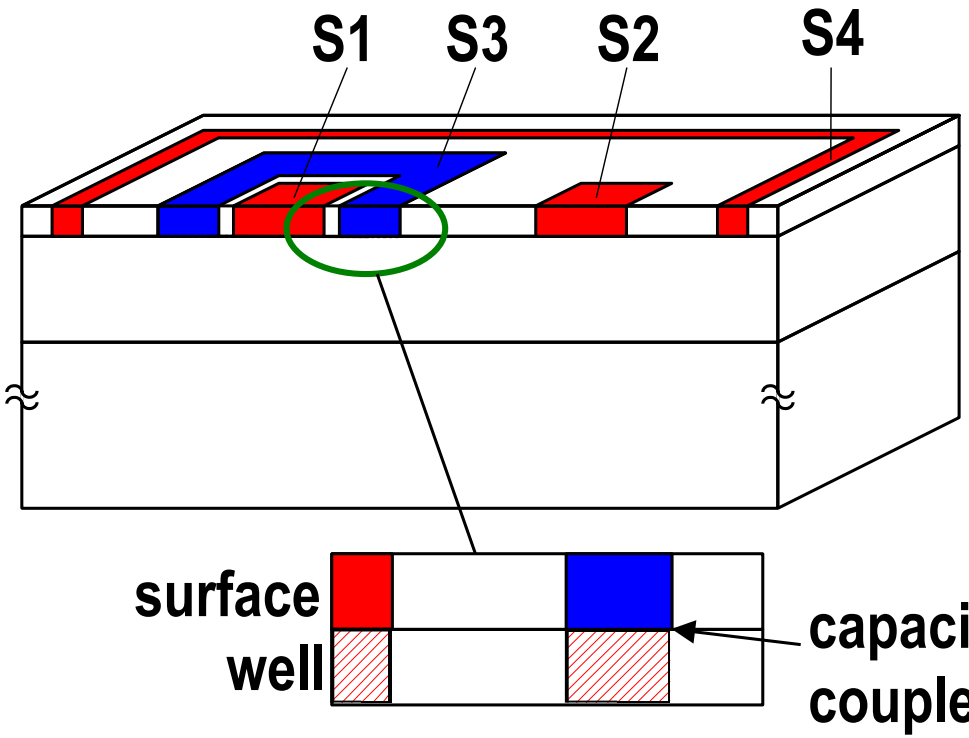
- Insert junction capacitances

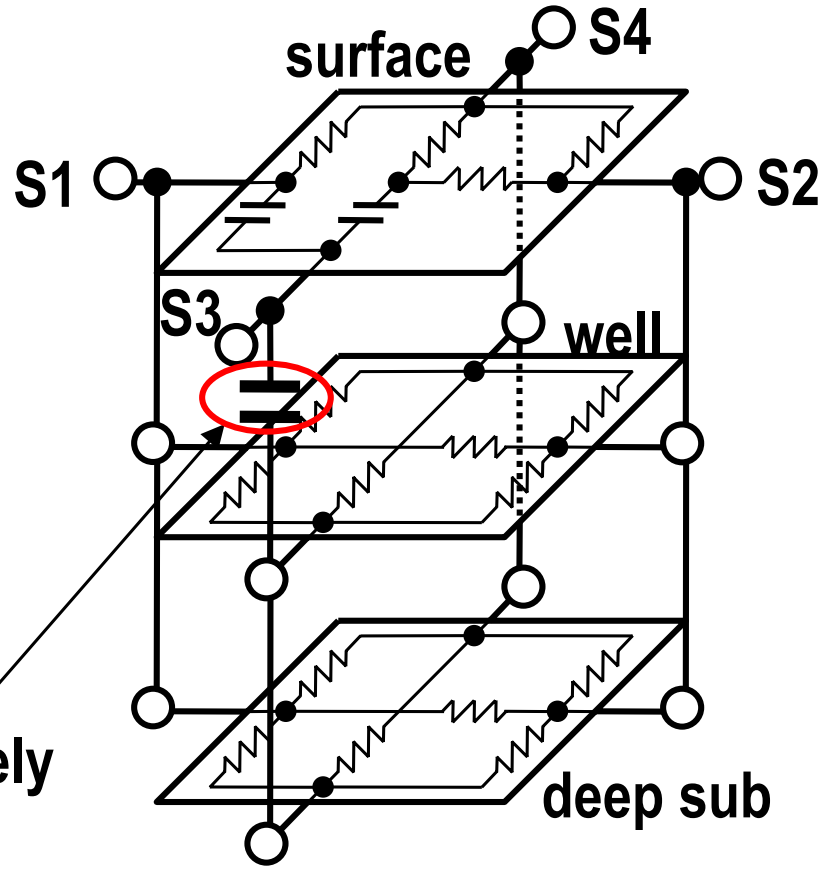




n+ guard ring

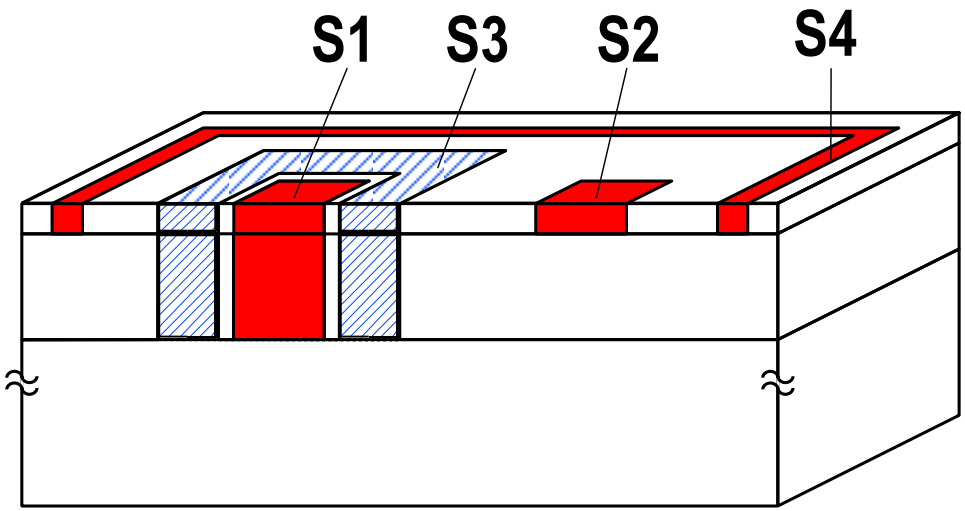
- Connect sub-models

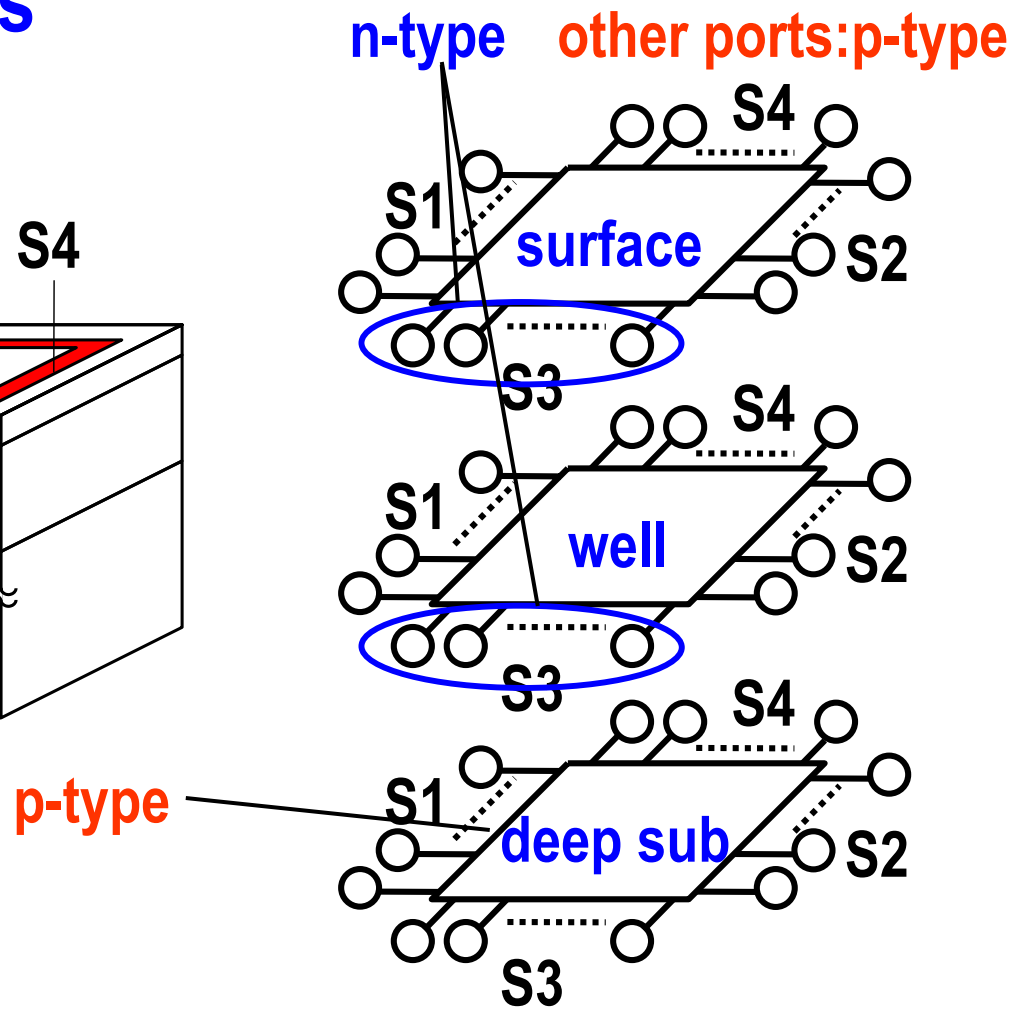




Deep n-well guard ring

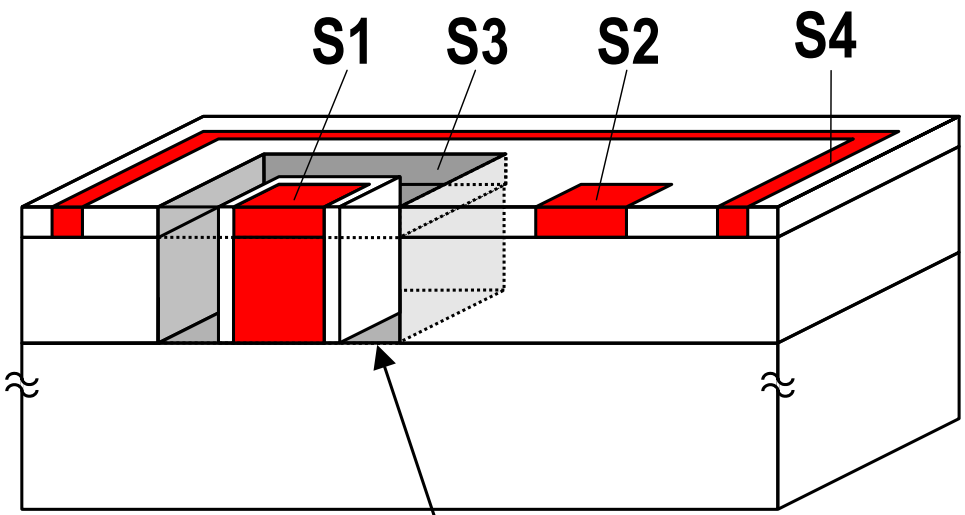
- Derive sub-models

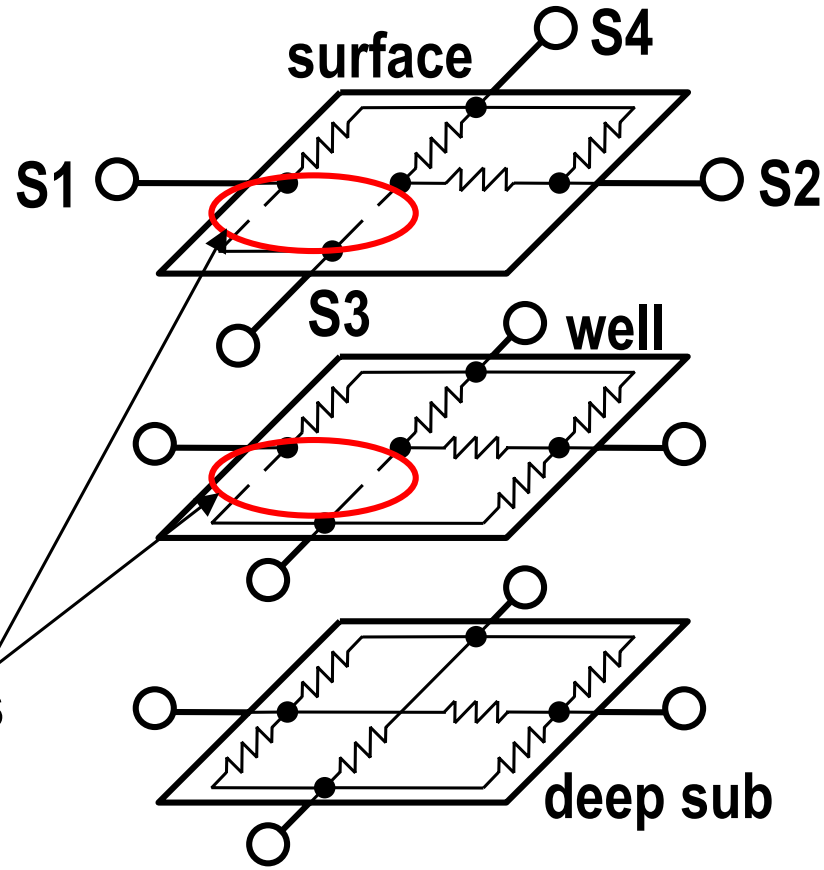




Deep n-well guard ring

- Short/cut observation points

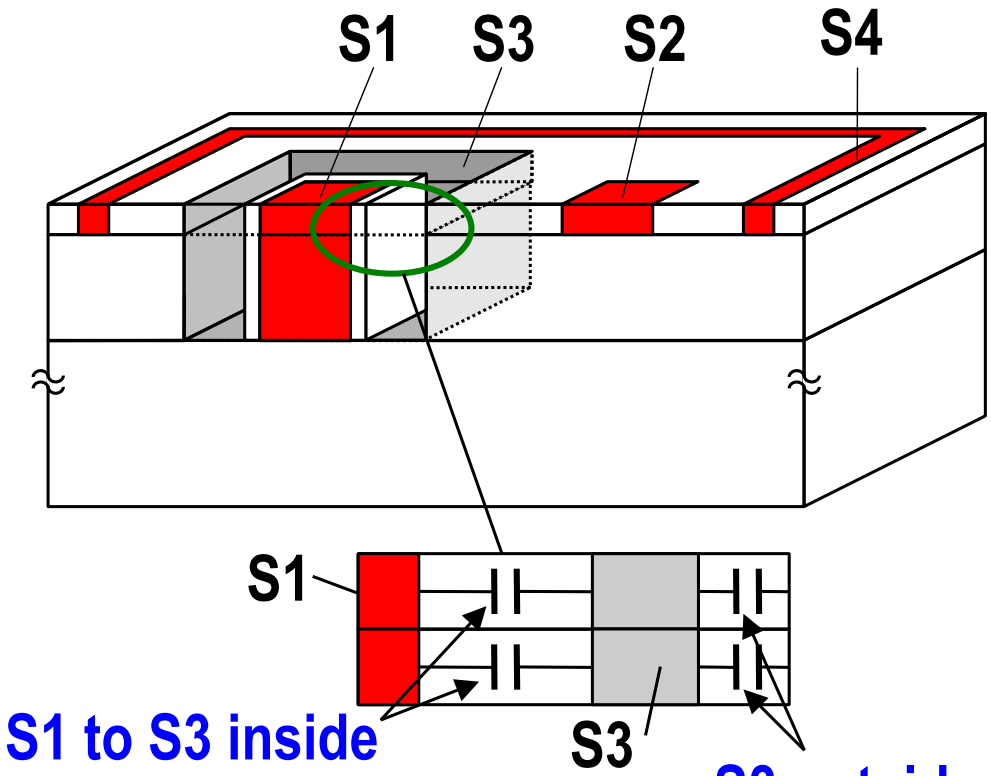


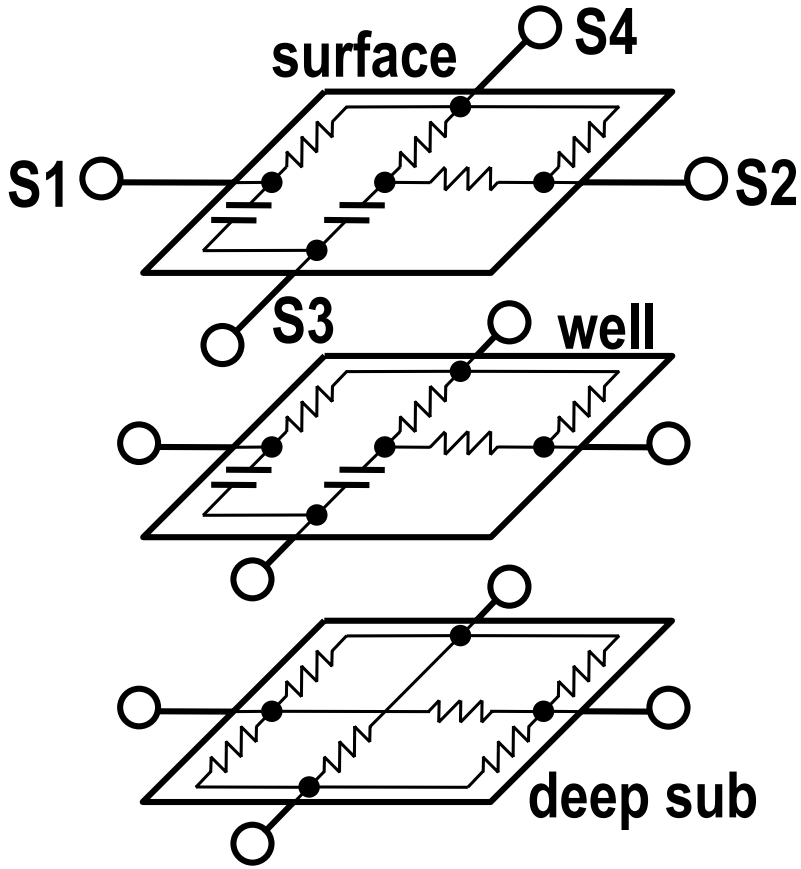


Cut observation points

Deep n-well guard ring

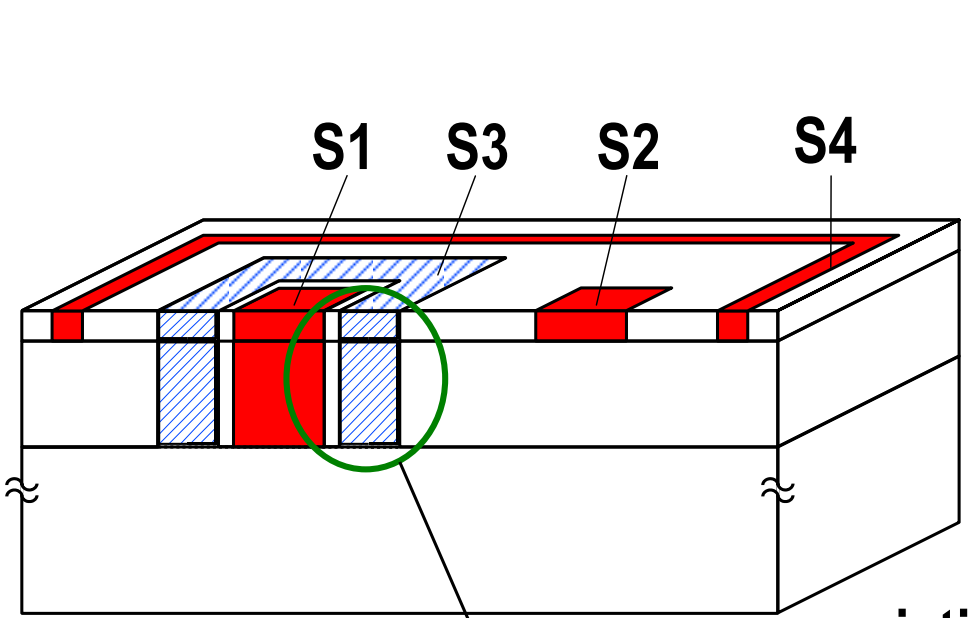
- Insert junction capacitances

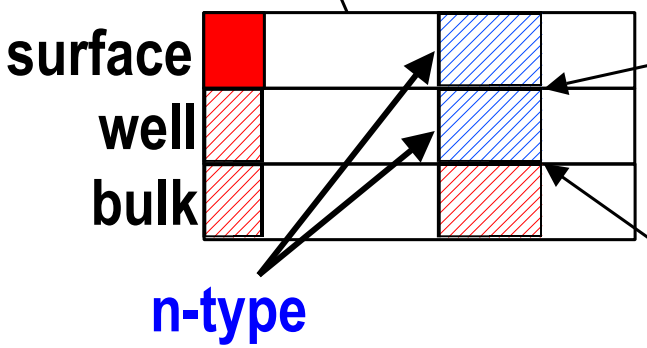




Deep n-well guard ring

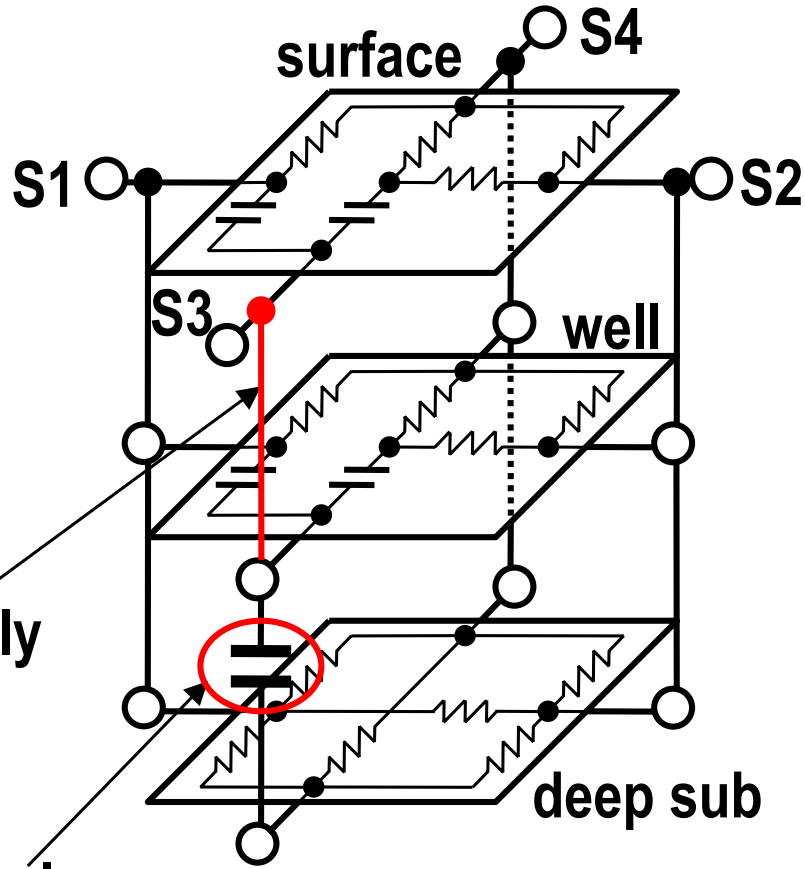
- Connect sub-models





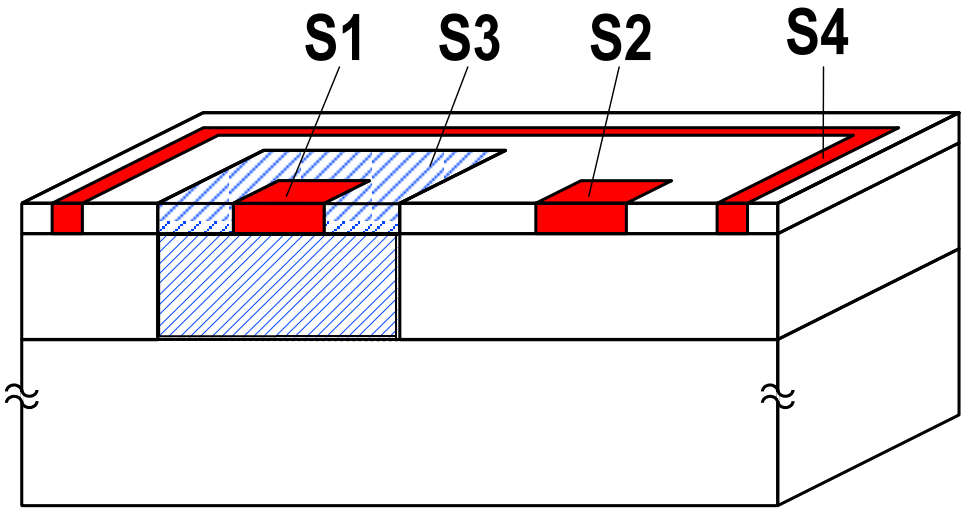
resistively coupled

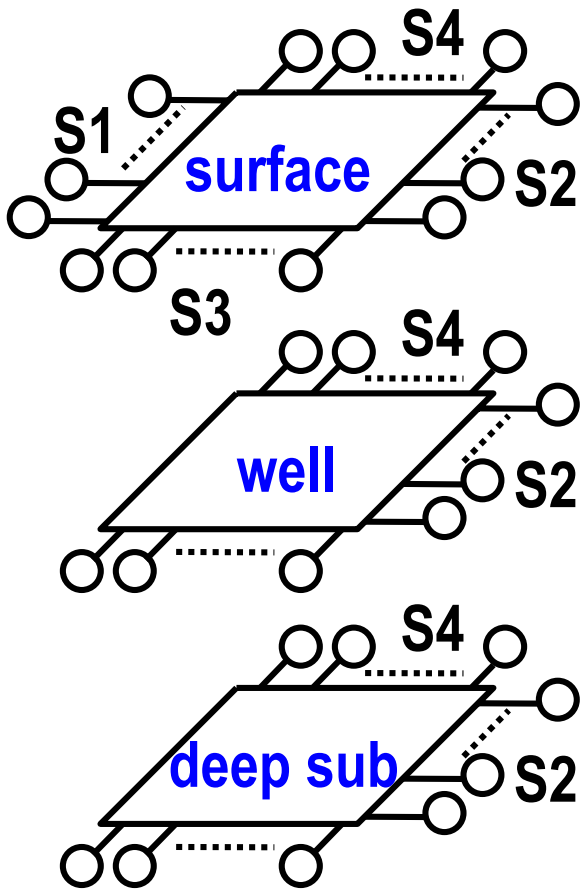
capacitively coupled



Deep n-well pocket

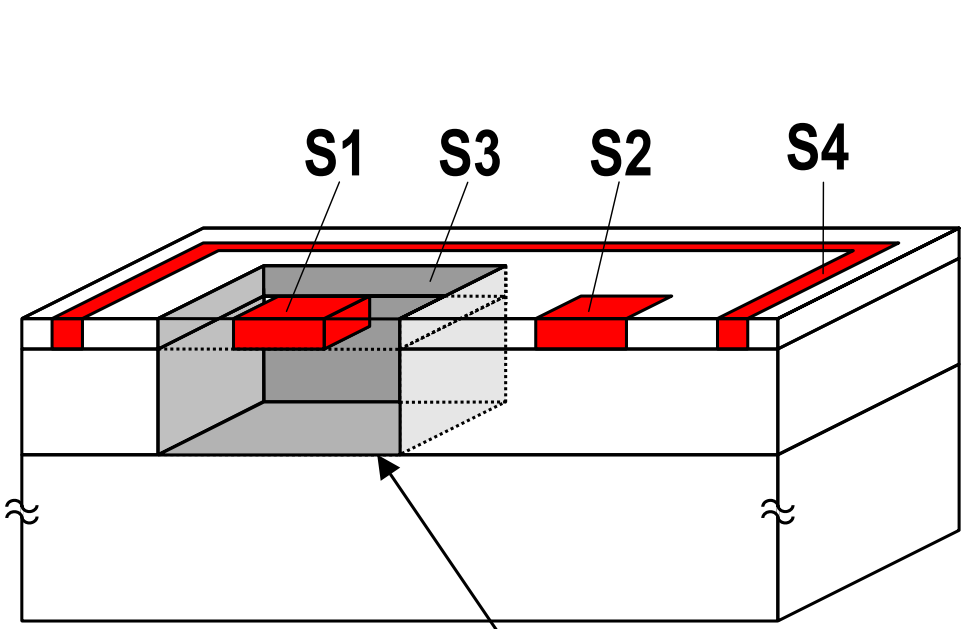
- Derive sub-models

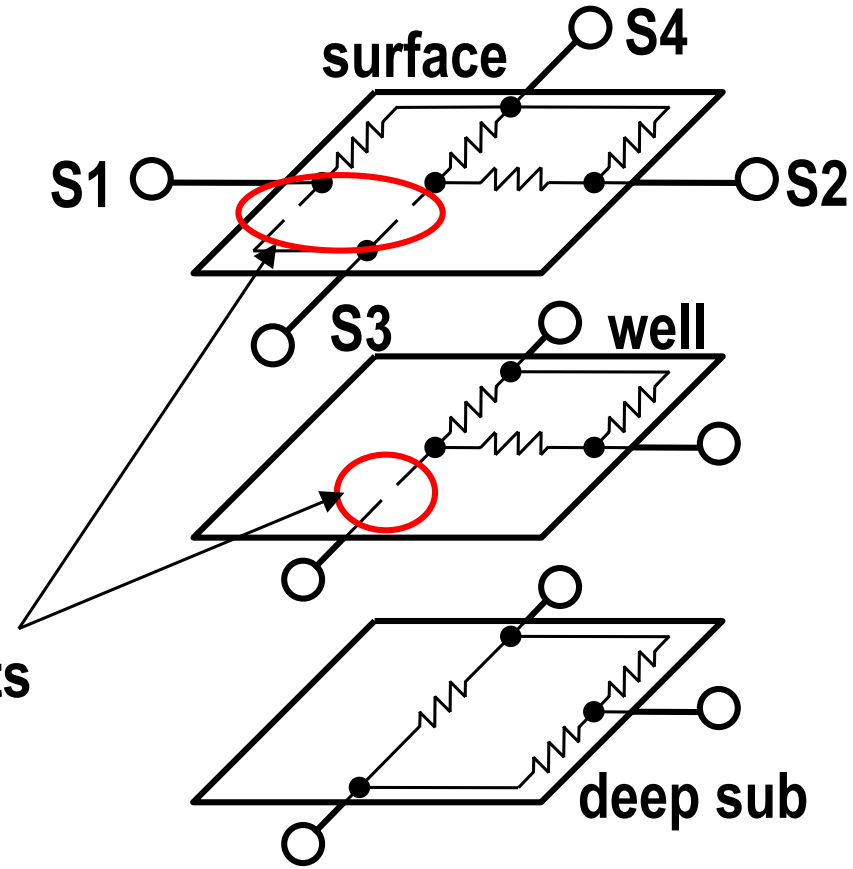




Deep n-well pocket

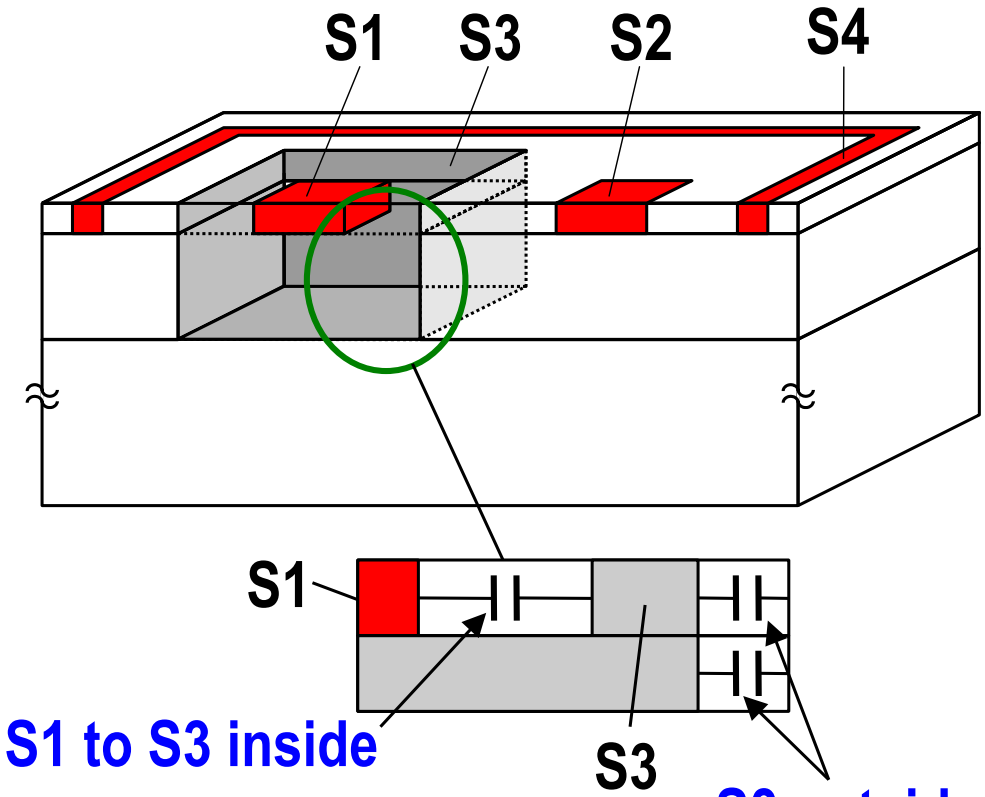
- Short/cut observation points

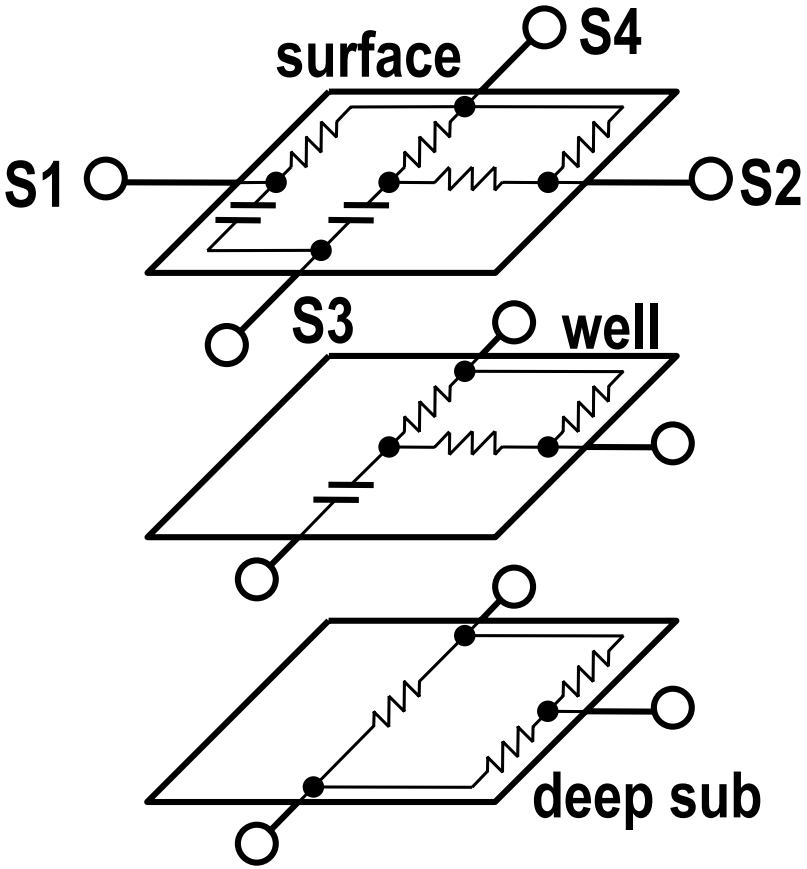




Deep n-well pocket

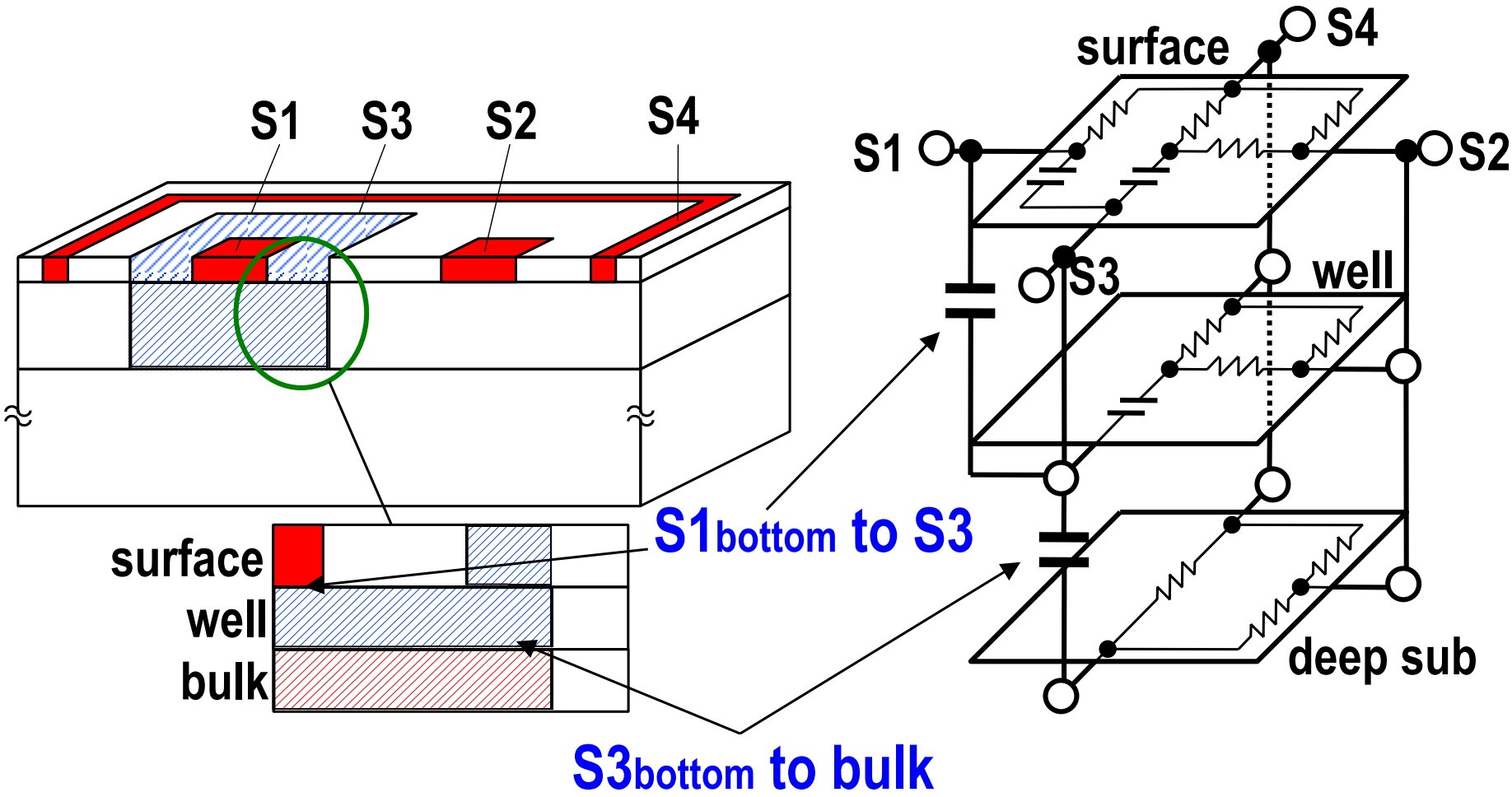
- Insert junction capacitances



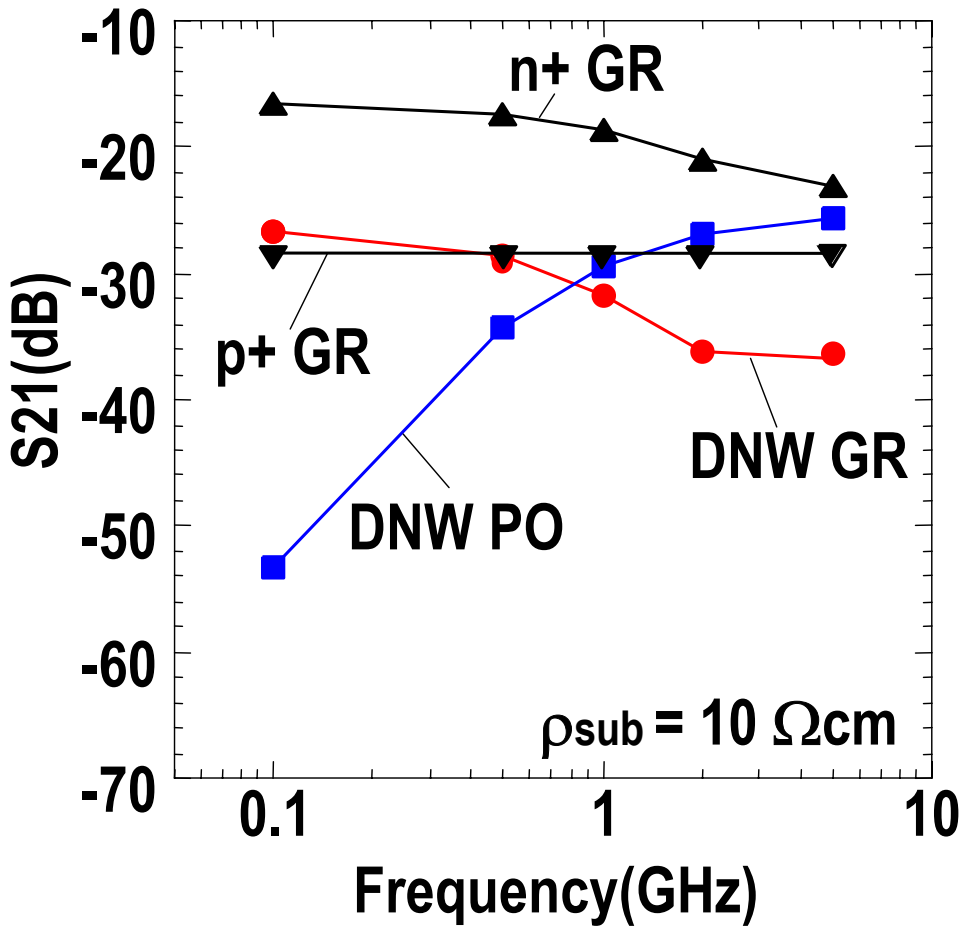


Deep n-well pocket

- Connect sub-models



Comparison with guard ring structures



effectiveness of each guard ring

p+ GR : constant isolation in all frequency areas

n+ GR : absorb and drain out current flowing in the substrate

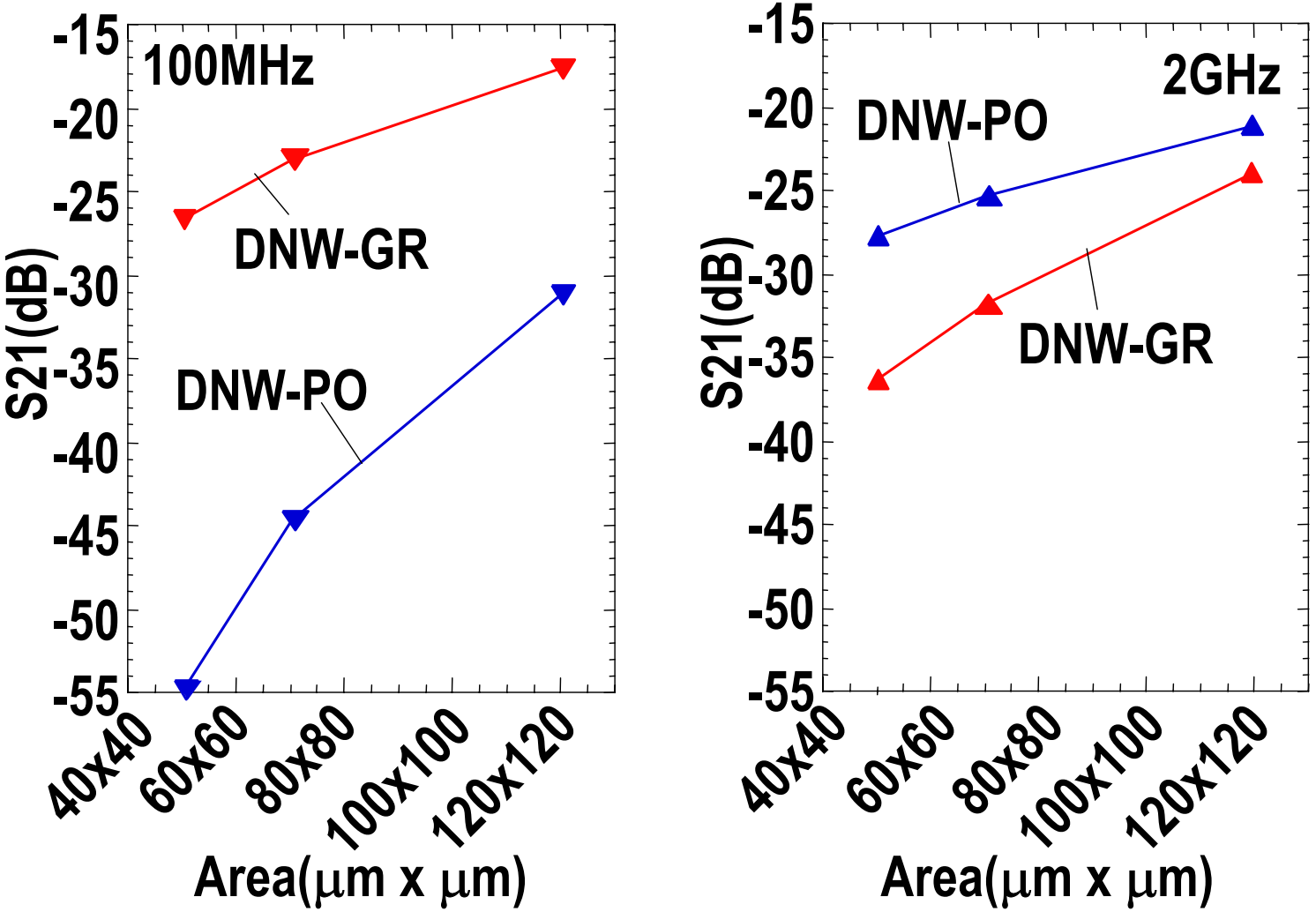
DNW GR : similar to **n+ GR**

--- high isolation in high frequency area

DNW PO : large bottom area

--- decrease impedance in high frequency area

DNW-GR vs. DNW-PO



Summary

- **Equivalent circuit model of RF isolation structures**
  - short/cut : express p/n diffusion(well)
  - 3-sub-models cascaded : express impurity profile
  - Computation time : 30min. for 240x240 mesh with 3 layers
- **Isolation strategy : Deep n-well GR**
  - DNW-GR cuts out high-conductive sheet formed by channel stop implant.

Strongly helpful to establish isolation strategy against substrate coupling

Acknowledgements

- *Atsushi Iwata, Yoshitaka Murasaka (A-R-Tec)*
- *Tetsuro Matsumoto (Kobe University)*