

# Floor Plan Noise Analysis Tool (FPNA)

## Application Example for Analog-RF Mixed Signal LSI

2009.12. 3

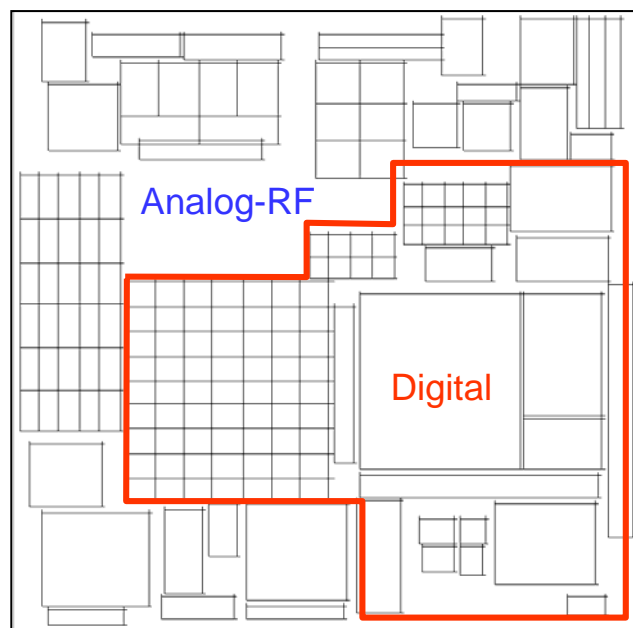
A-R-Tec

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## GDS & Floor Plan of Simulation Example LSI

Mixed Signal (Analog, RF, Digital) CMOS LSI

Floor Plan (FP0905)



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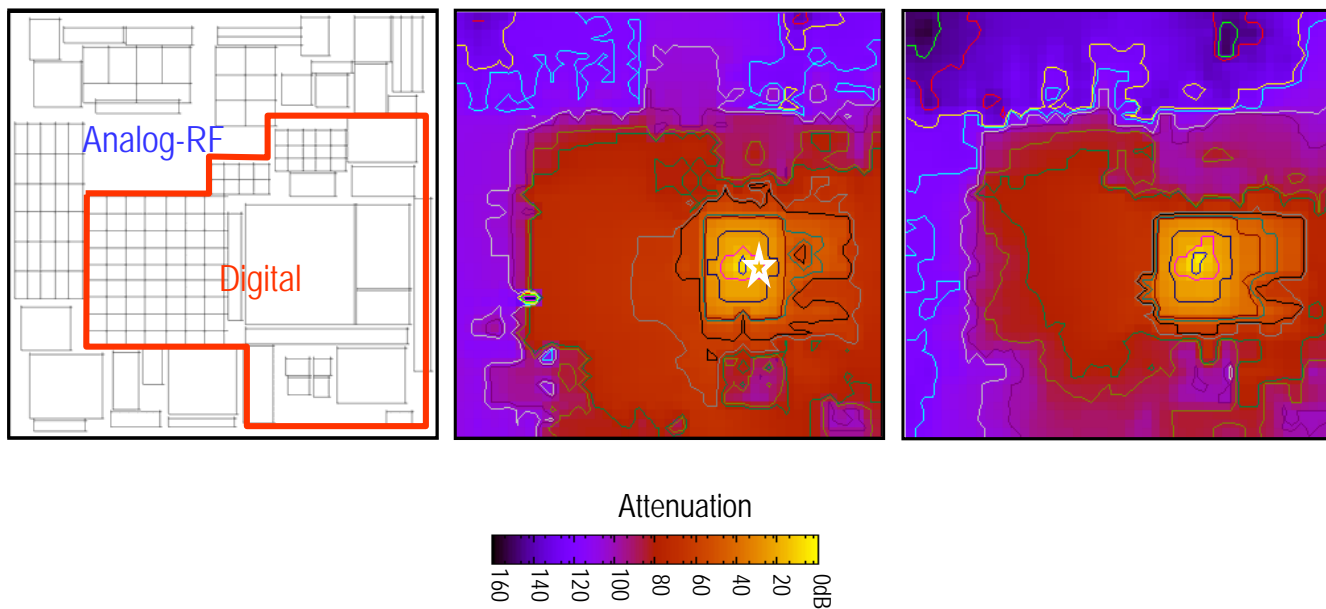
# Simulated PSUB Noise Attenuation Map

Noise Source: PSUB in Digital Block, Noise Frequency=DC

Floor Plan (FP0905)

Floor Plan based

GDS based



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# Simulated PSUB Noise Attenuation Map

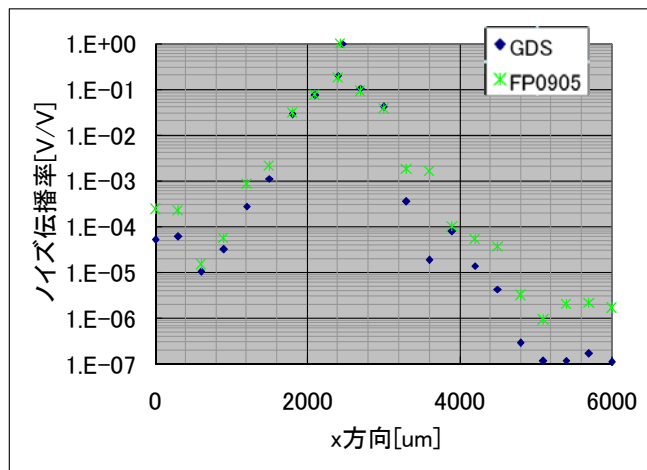
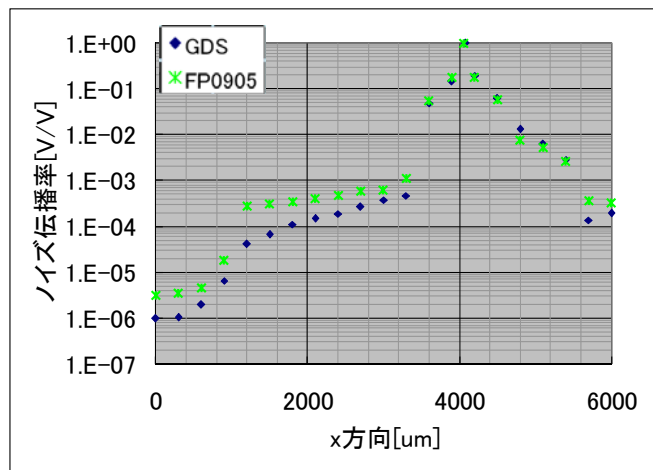
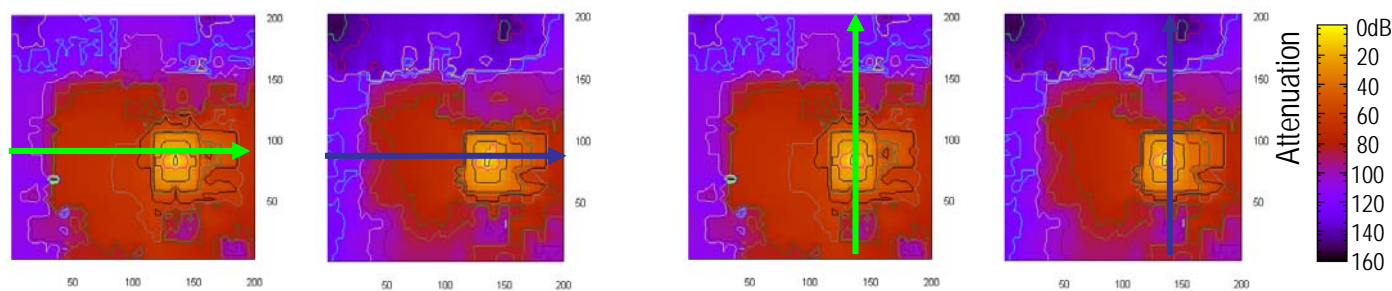
Noise Source: PSUB in Digital Block, Noise Frequency=DC

FP0905

GDS

FP0905

GDS



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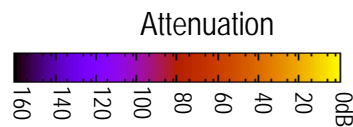
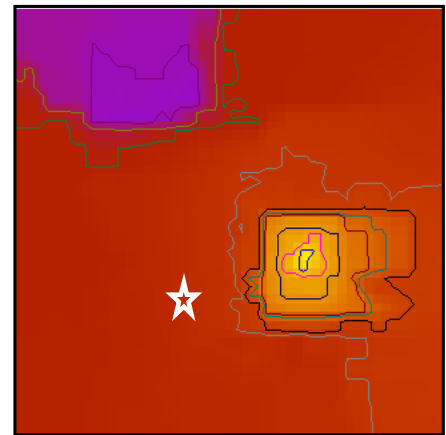
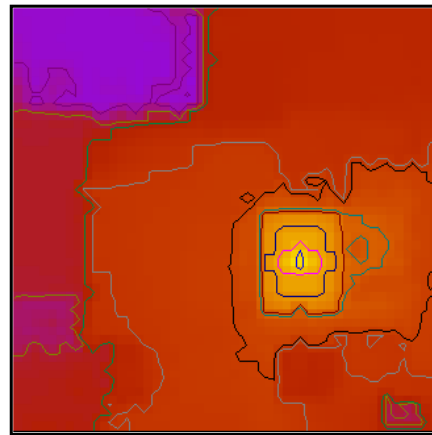
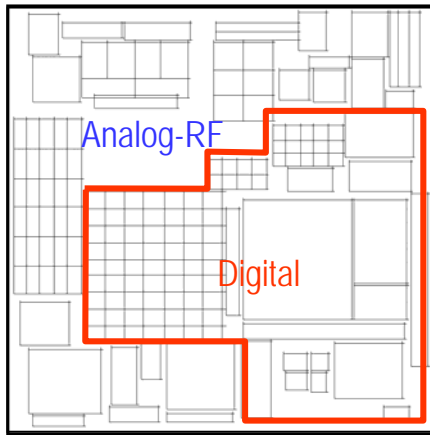
# Simulated PSUB Noise Attenuation Map

Noise Source: PSUB in Digital Block, Noise Frequency=2GHz

Floor Plan (FP0905)

Floor Plan based

GDS based



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# Simulated PSUB Noise Attenuation Map

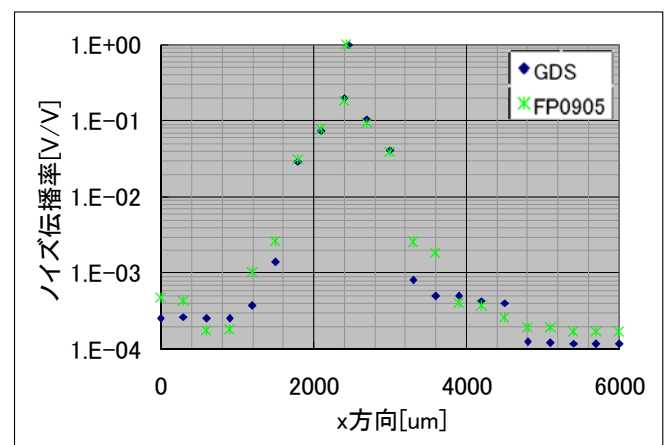
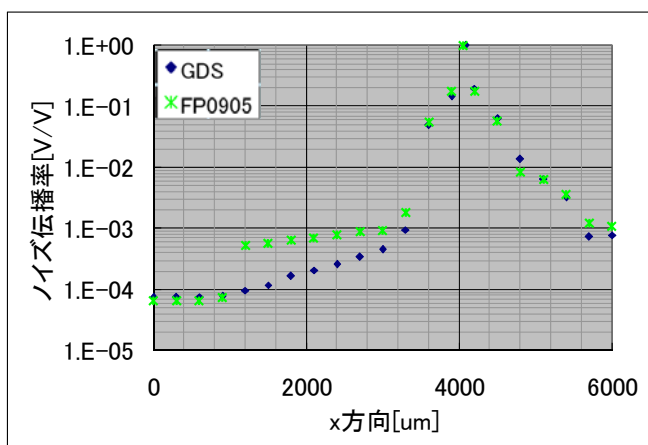
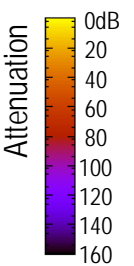
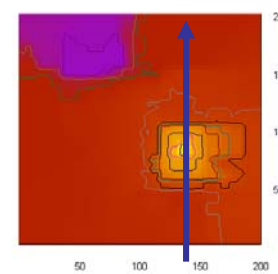
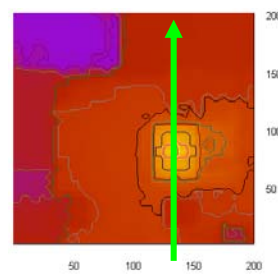
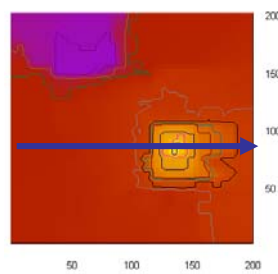
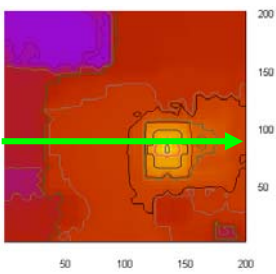
Noise Source: PSUB in Digital Block, Noise Frequency=2GHz

FP0905

GDS

FP0905

GDS

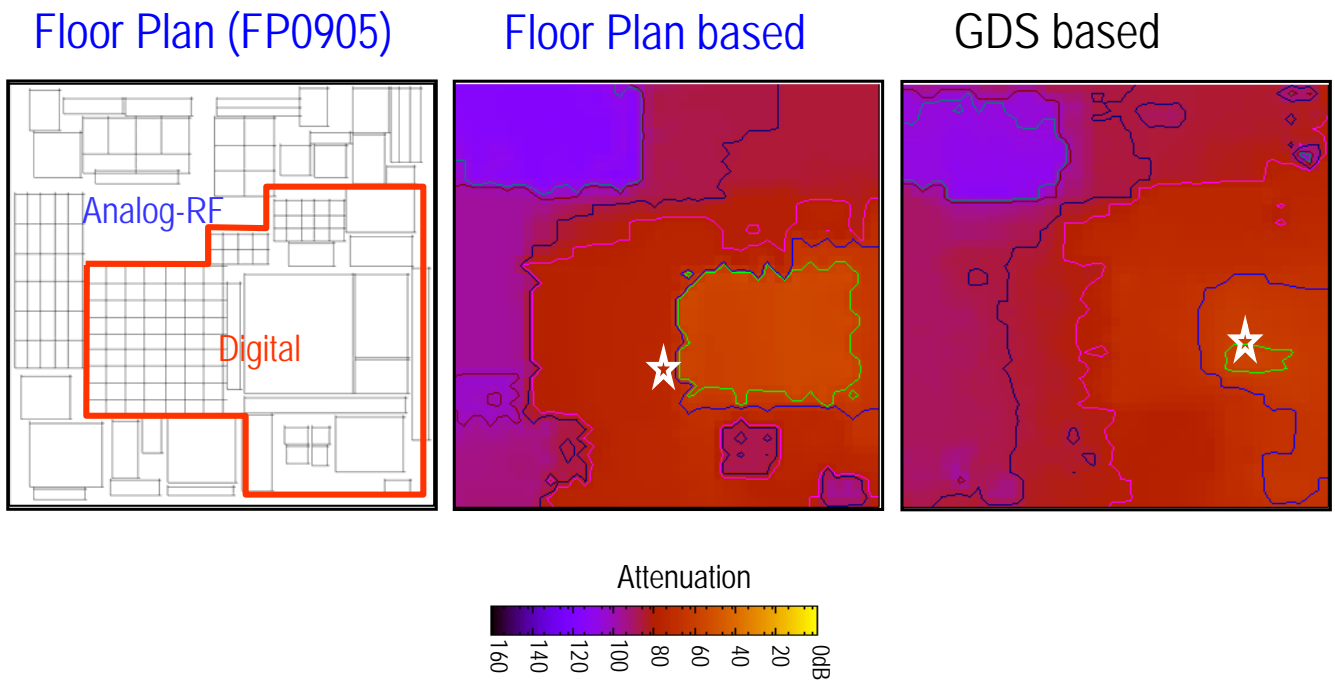


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# Simulated PSUB Noise Attenuation Map

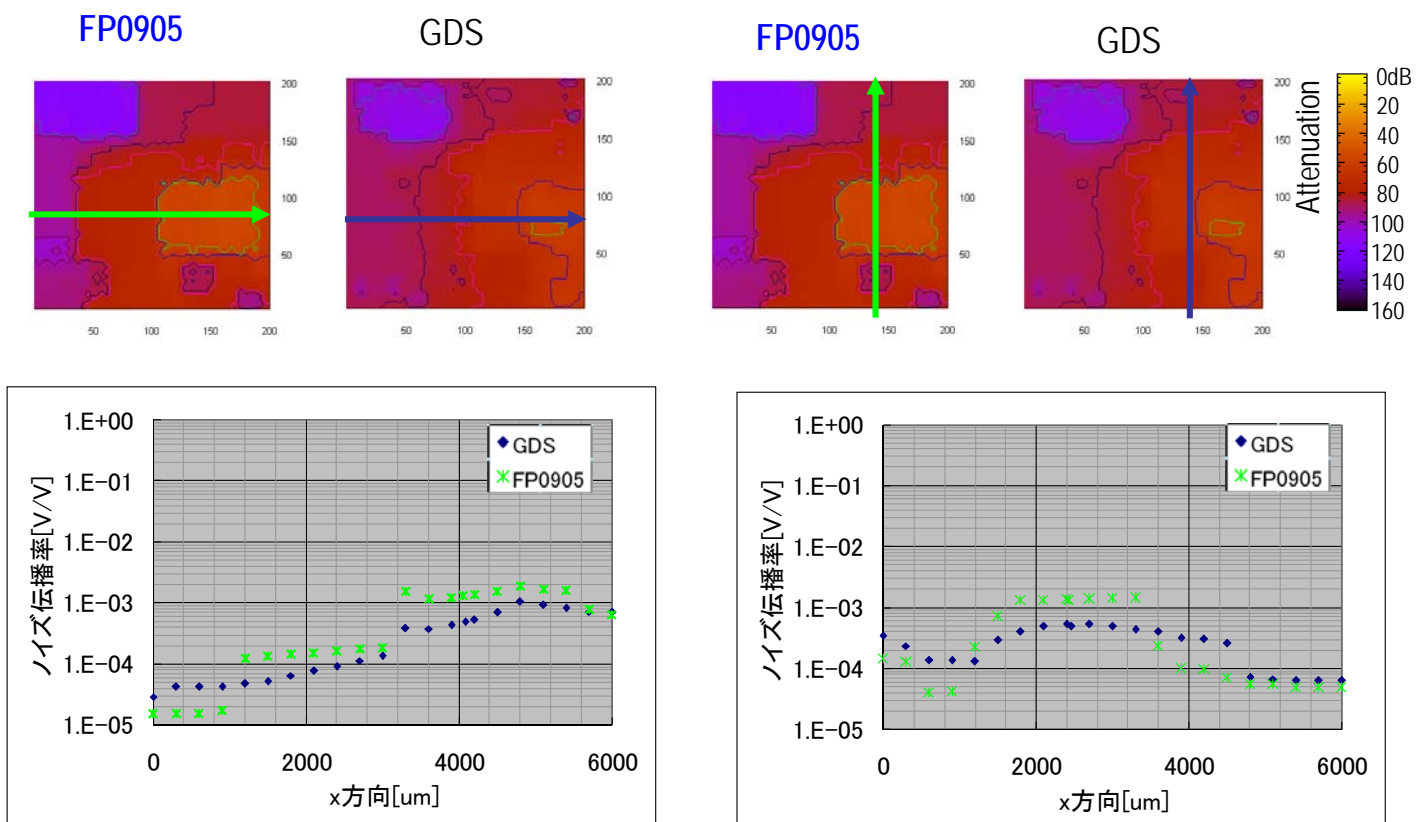
Noise Source: Deep-Nwell in Digital Block, Noise Frequency=2GHz



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# Simulated PSUB Noise Attenuation Map

Noise Source: Deep-Nwell in Digital Block, Noise Frequency=2GHz

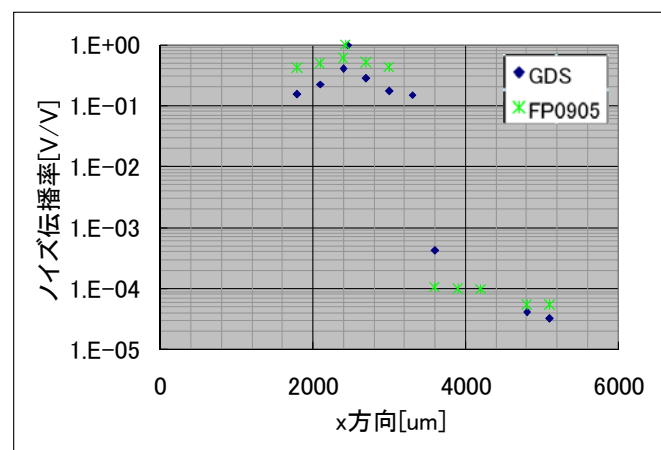
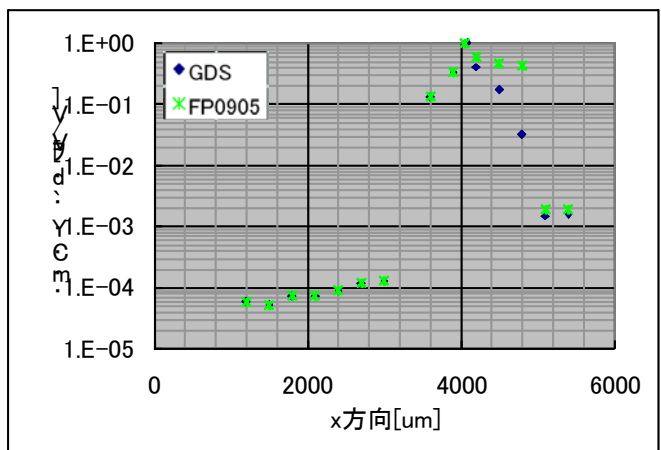
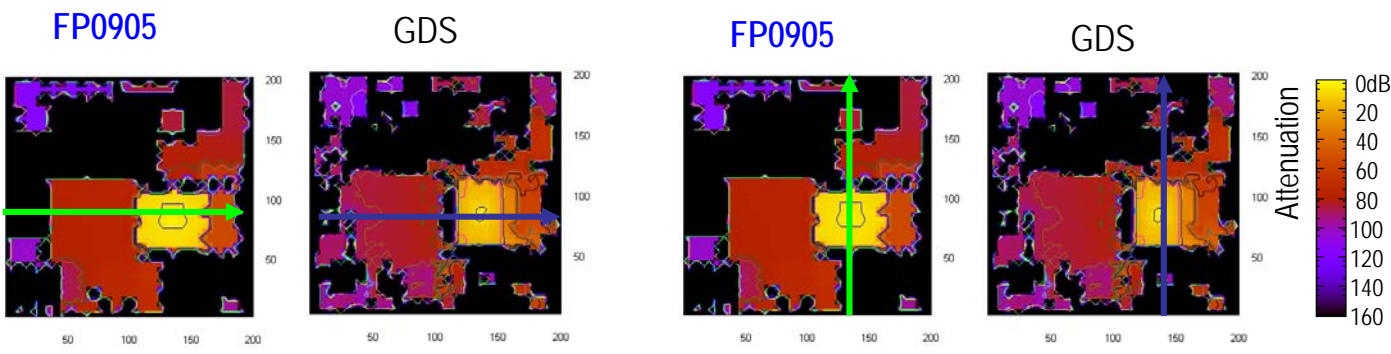


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# Simulated Deep-Nwell Noise Attenuation Map

Noise Source: Deep-Nwell in Digital Block, Noise Frequency=2GHz

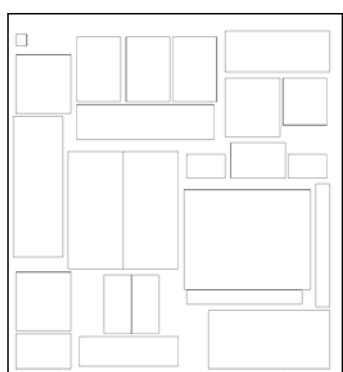


## FPNA 処理時間例

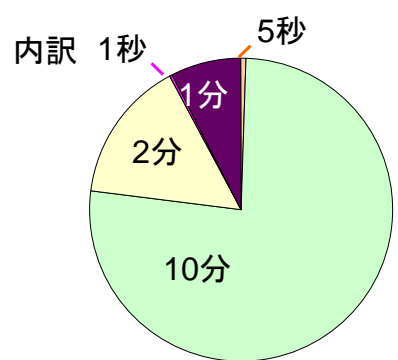
解析対象例 : RFCMOSフロアプラン  
 モデル化対象 : PSUB, 基板コンタクト, M1(G.R.配線)  
 計算機仕様 : CPU:( AMD Opteron Freq: 2.7GHz  
                   Cash:512KB)  
                   Memory: 32GB  
 シミュレータ : Smart Spice (SILVACO社)  
 解析内容 : DC解析,  
             AC解析ノイズ源の周波数26MHz  
                   76.8MHz  
                   245.76MHz  
                   2GHz

RFCMOS フロアプラン例

■ 処理時間: 約13分



回路ブロック数24個(G.R.配線数24個)



- 入力データ取得 ~ ネットリスト作成
- Fmatrix演算
- シミュレーション
- データ抽出
- 波形表示